CH32M030 Datasheet

V1.1

Overview

CH32M030 series is an industrial-grade motor microcontroller designed based on QingKe RISC-V3B core. CH32M030 has built-in 4 OPAs and 3 CMPs, which support combining into 2 sets of AC small-signal amplification decoder QII and 2 sets of differential input current sampling ISP; built-in USB PHY and PD PHY, which support USB Host and USB Device function, PDUSB, Type-C fast charging function, BC1.2 and DCP/CDP and other high-voltage charging protocols; built-in 4 pairs of N-type power tubes gate pre-driver, to provide high-voltage I/O; built-in programmable current-flooding module; to provide DMA controller, 12-bit ADC, multi-group timer, UART serial port, I2C, SPI and other peripherals resources, provide over-voltage protection and over-temperature protection.

Features

- **Core**
  - QingKe 32-bit RISC-V core
  - Support RV32IMCB instruction set and self-expanding instruction.
  - 3-stage pipeline
  - Unique high-speed interrupt response mechanism
  - Maximum 72MHz system frequency
- **Memory**
  - 12KB volatile data storage area SRAM
  - 64KB Code Flash with ECC program storage area
  - 512B user-defined storage area
- **Power management and low-power consumption**
  - Built-in high-voltage LDO, V_{HV} supports rated 5~28V system power supply.
  - Predrive I/O supply V_{DD8} Rated voltage: 5~10V
  - General I/0 and ADC supply V_{DD33} rated voltage: 3.3V
  - Low-power mode: Sleep, Stop, Standby
- **4 dual N-type MOSFET half-bridge driver**
  - 4 pairs of high side/low side MV pins, supporting V_{DD8} voltage.
  - Built-in low voltage drop bootstrap diode, only external capacitor is needed.
  - Can be combined into three-phase motor grid drive.
  - Can be combined into 2 independent full-bridge drives.
- **System clock**
  - Built-in factory-adjusted 8MHz RC oscillator
  - Built-in RC oscillator of about 340kHz
  - Support external 4 ~ 25mhz crystals.
- **7-channel general DMA controller**
  - 7 channels, supporting ring buffer management
  - Support TIMx/ADC/UART/I2C/SPI
- **12-bit ADC**
  - Analog input range: GND~V_{DD33}
  - 20-channel external signals
  - Support external delay trigger and ADC moving average function.
- **OTP, OVP and under-voltage reset.**
- **UART with multi-pin mapping**
- **I2C interface**
- **SPI interface**
- **2 sets of Type-C, USB PD controller and PHY**
  - Support DRP, Sink and Source application
  - 4 high-voltage tolerant CC pins
- **Full-speed USB 2.0 controller and PHY**
  - Supports PDUSB, Host and Device modes.
  - Supports BC1.2 and various HV DCP/CDP charging protocols.
  - Built-in 6-bit DAC, programmable voltage output and pull-up/down.
- **Multiple timers**

- 16-bit advanced-control timer, with dead zone control and emergency brake; can offer PWM complementary output for motor control
- 16-bit general-purpose timer
- 16-bit streamlined general-purpose timer
- Window watchdog timer
- SysTick: 32-bit counter

- **4 OPAs and 3 CMPs**
  - Can be combined as 2 sets of AC small-signal amplification decoders QII1 and QII2 and 2 sets of differential input current sampling ISP1 and ISP2
  - OPA1 and OPA2 support self-biased PGAs.
  - OPA3 and OPA4 support single-ended and differential inputs, PGA multi-step gain selection, and provide internal self-biasing voltage.
  - CMP1 supports digital filtering
  - CMP2 and CMP3 support N-terminal bias selectable, digital filtering
  - CMP3 has multiple input channels, output to I/O or internal
- **2 sets of 10-bit programmable flood current module**
- **2 sets of source current module**
- **GPIO**
  - 36 GPIO ports, mapping 16 external interrupts
  - 8 MV pre-drive pins, 2 HV high voltage pins
- **Security features: Chip unique ID**
- **Debug mode:**
  - **Support 1-wire and 2-wire serial debug interface (SDI)**
- **Package: LQFP, QFN, QSOP**

Resource \ Model		C8U3	C8T7	C8U7	K8U7	G8R7
Chip pin number		48	48	48	32	28
Code Flash (byte)		64K	64K	64K	64K	64K
SRAM (byte)		12K	12K	12K	12K	12K
Half-bridge gate driver		4	4	4	2	3
GPIO		36	35	36	24	17
Pre-drive I/O (MV I/0)		8	8	8	6	6
High voltage I/O（HV I/0）		2	-	1	1	-
Timer	Advanced-control TIM1 (16-bit)	1	1	1	1	1
	General-purpose TIM2 (16-bit)	1	1	1	1	1
	Streamlined TIM3 (16-bit)	1	1	1	1	1
	WWDG	1	1	1	1	1
	System time base (32-bit)	√				
ADC		20	20	20	16	11
OPA1		1	1	1	-	-
OPA2		1	1	1	1	1
OPA3		1	1	1	1	1

OPA4			1	1	1	1	1
CMP1			1	1	1	-	-
CMP2			1	1	1	1	1
CMP3			1	1	1	1	1
Current sampling ISP, ISN			Differential*2	Differential *2	Differential *2	Differential *1 Single end*1	Differential *2
Signal decoding QII			2	2	2	1	1
Programmable current injection module ISINK			2	2	2	2	1
Source current module ISOURCE			2	2	2	1	-
Communication interface	UART		1	1	1	1	1
	SPI		1	1	1	1	-
	I2C		1	1	1	1	1
	PDUSB	USBFS	Host Device	Host Device	Host Device	Host Device	Host Device
		USB PD Type-C	(CC1R, CC2R) (CC3, CC4) Built-in Rd(1)	(CC1, CC2) (CC3, CC4)	(CC1R, CC2R) (CC3, CC4) Built-in Rd(1)	(CC1R, CC2R) (CC3, CC4) Built-in Rd(1)	(CC3, CC4)
Package form			QFN48X7_A	LQFP48	QFN48	QFN32	QSOP28

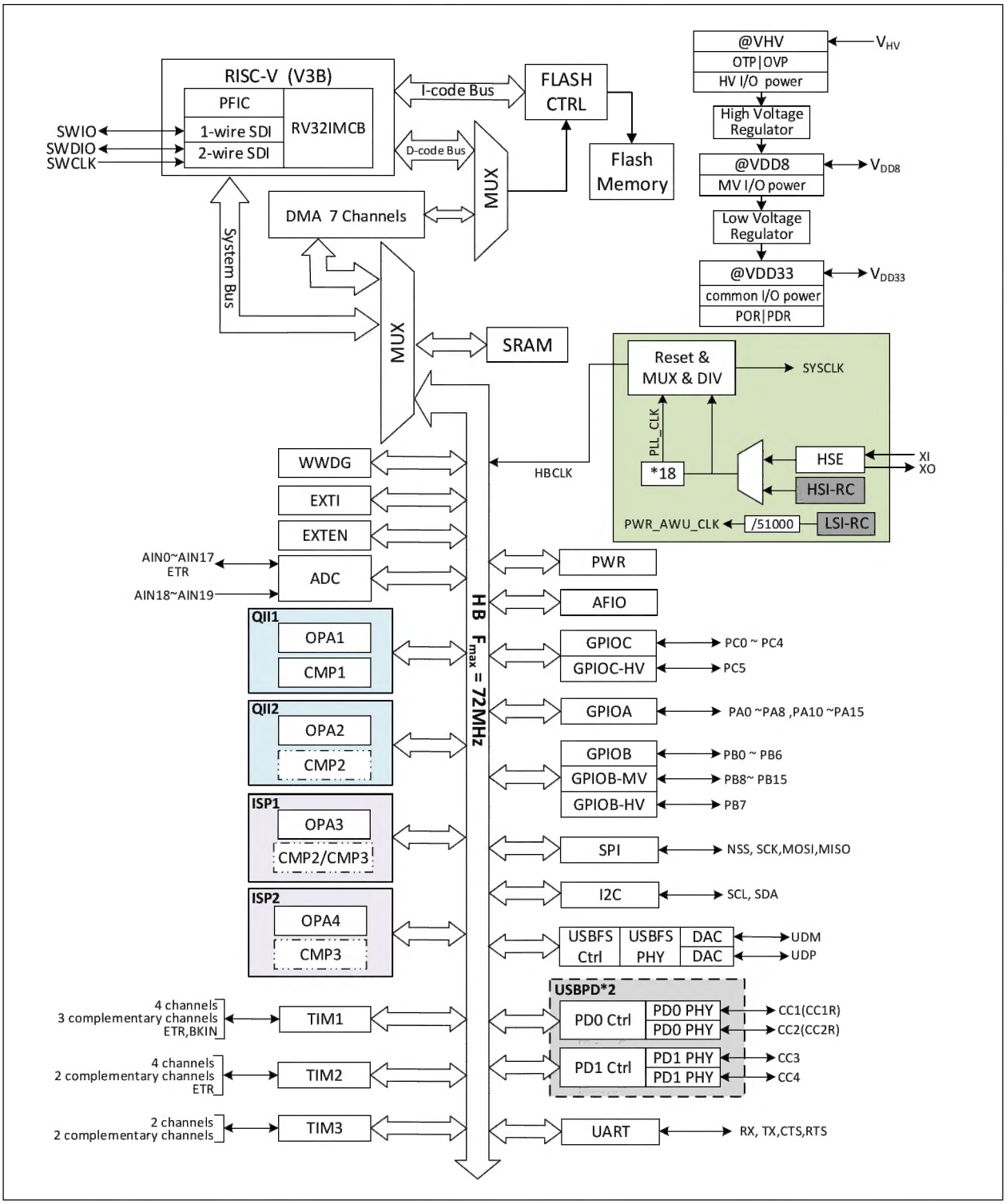
Note: 1. Pins PA0/CC1R and PA1/CC2R have built-in Type-C specification-defined controllable Rd pull-down resistors of approximately 5.1kΩ.

Chapter 1 Specification Information

1.1 System Structure

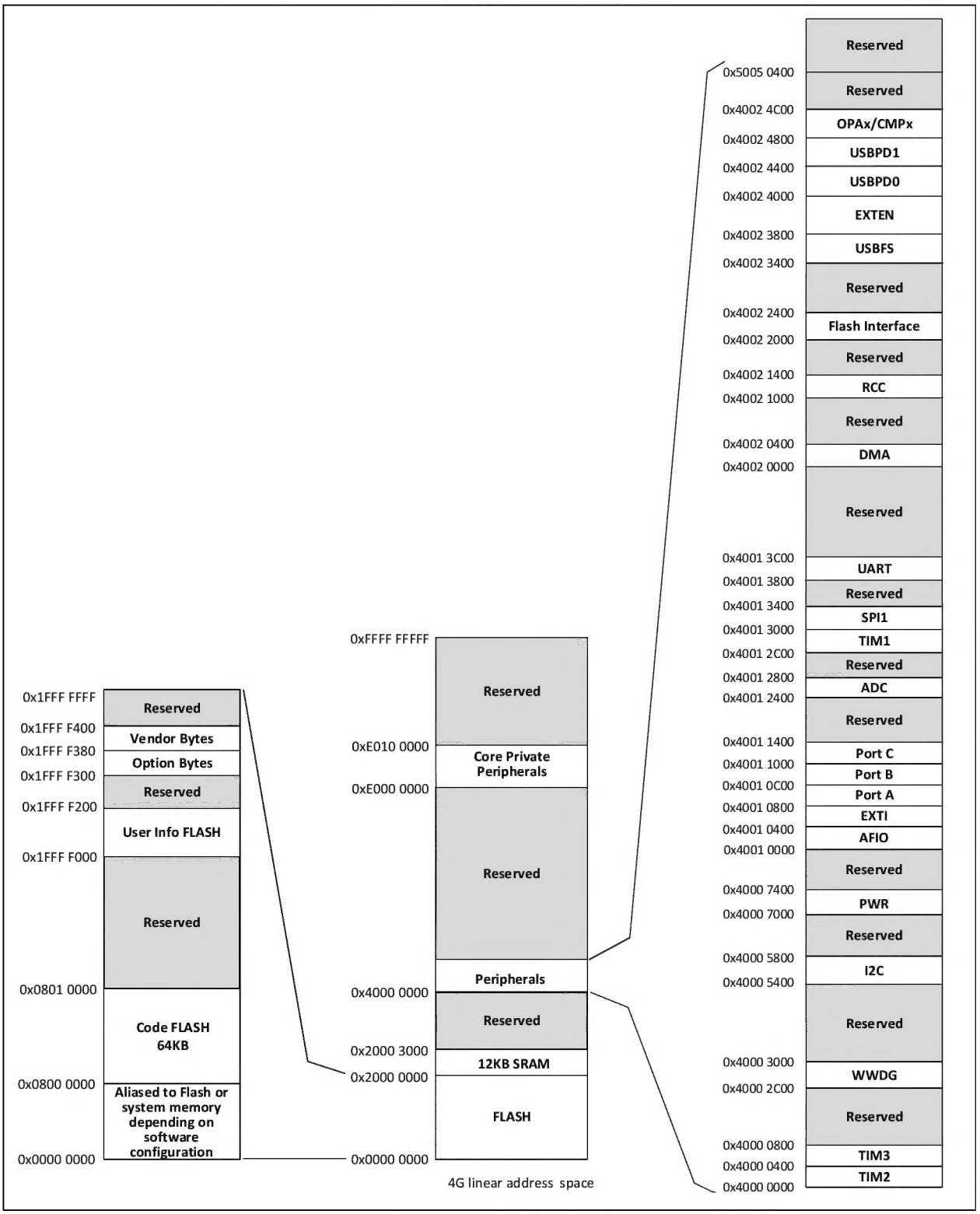
The microcontroller is based on the QingKe V3B design of the RISC-V instruction set, and its architecture realizes the interaction of the core, the arbitration unit, the DMA module, the SRAM storage, and other parts through multiple sets of buses. The design integrates a general-purpose DMA controller to reduce the burden on the CPU, improve access efficiency. Multi-level clock management mechanism is applied to reduce the power consumption of peripherals, while both data protection mechanisms, automatic clock switching protection and other measures to increase system stability. The following diagram shows the CH32M030 internal overall architecture.

Figure 1-1 System block diagram



1.2 Memory Map

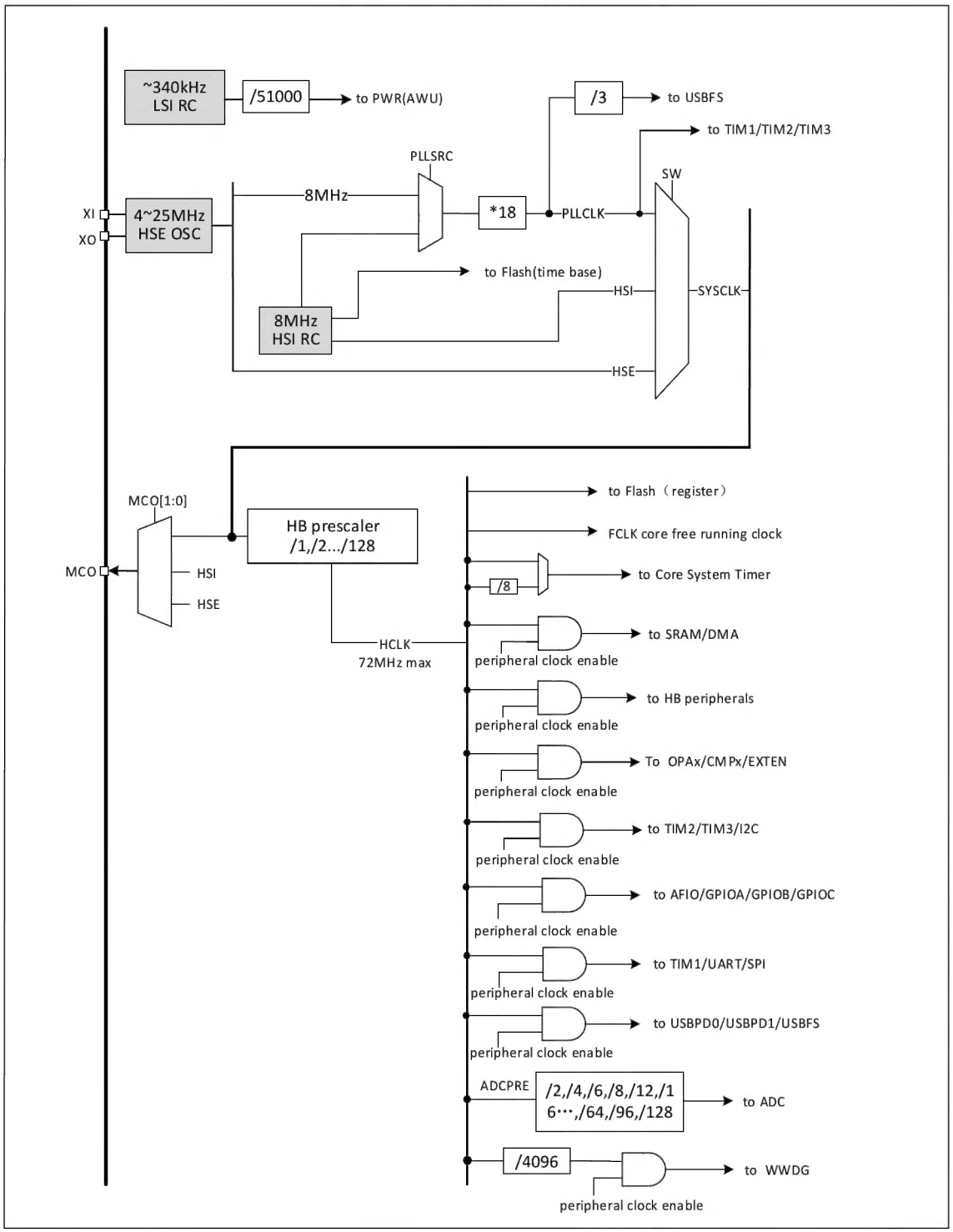
Figure 1-2 Memory address map



1.3 Clock Tree

3 sets of clock sources are introduced into the system: Internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI) and external high-frequency oscillator (HSE). Among them, the low-frequency clock source provides a clock reference for the automatic wake-up unit, and the high-frequency clock source is directly or indirectly output as the system bus clock (SYSCLK) through a 18x multiplier, and the system clock is then provided by the pre-scaler for the HB domain peripheral control clock and sampling or interface output clock. Part of the module working need to be provided by PLL clock directly.

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V3B Processor

RISC-V3B supports RISC-V instruction set EmC[1] subset. The processor is internally managed in a modular fashion and contains units such as a programmable fast interrupt controller (PFIC), extended instruction support, and so on. The bus is connected to external unit modules to enable interaction between external function modules and the core.

QingKe processor with its minimalist instruction set, a variety of operating modes, modular customization and expansion features can be flexibly applied to different scenarios MCU design, such as small area low-power embedded scenarios.

- Support machine and user privileged modes
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- Support 1-wire /2-wire serial debug interface (SDI)
- Custom extension instructions

1.4.2 On-chip Memory

Built-in 12K-byte SRAM area, which is used to store data, which is lost after power loss.

Built-in 64K-byte program flash memory area (Code FLASH), that is, the user area, is used for users' applications and constant data storage.

Built-in 512-byte user-defined information storage area (User Info FLASH), operable only with the WCH-LinkUtility software tool.

Built-in 128-byte system non-volatile configuration information storage area, used for manufacturer configuration word storage, solidified before leaving the factory, users can not be modified.

Built-in 128-byte user-defined information store for user option byte storage.

1.4.3 Power Supply Scheme

CH32M030 has built-in 3-stage LDO regulators, namely, a high-voltage regulator generating V_{DD8} from V_{HV}, a low-voltage regulator generating V_{DD33} from V_{DD8}, and a core regulator generating core power from V_{DD33}.

V_{HV} = 4.0~29.0V: To supply power to the internal high voltage regulator and HV high voltage I/O pin, it is recommended that the accumulated capacitance on V_{HV} should not be less than 10uF.

V_{DD8} = 4.0~10.5V: The internal high voltage regulator generates voltage at the V_{DD8} pin, which supplies power to the MV pre-drive I/O pin and the internal low voltage regulator. It is suggested that V_{DD8} should be externally connected with 10uF decoupling capacitor; When the motor pre-drive is not enabled, the external capacitance can be reduced.

V_{DD33} = 3.1~3.5V: The internal low-voltage regulator generates a rated voltage of 3.3V at the V_{DD33} pin, which supplies power to the common I/O pin, ADC and core regulator. It is suggested that V_{DD33} be externally connected with a capacitor with a capacity of 1uF~10uF.

When working under high voltage, the accumulated power consumption of LDO in CH32M030 is large. In order to reduce the chip temperature, external power supply can be selected to directly supply 5.0~10.0 V to V_{DD8}. At this time, $V_{DD8} \leqslant V_{HV}$; is required; Externally, it is optional to directly supply 3.3V to V_{DD33}. At this time, $V_{DD33} \leqslant V_{DD8} \leqslant V_{HV}$ is required.

1.4.4 Protection and Reset Circuit

CH32M030 has integrated power-on reset (POR)/ power-off reset (PDR) circuit. When the voltage of V_{DD33} is higher than the set threshold ($V_{POR/PDR}$), the system starts to work. When the voltage of V_{HV} drops to make the voltage of V_{DD33} lower than the set threshold ($V_{POR/PDR}$), the system is placed in a reset state without using an external under-voltage reset circuit. Refer to Table 3-4 for the value of $V_{POR/PDR}$.

CH32M030 has built-in OTP over-temperature protection, which will forcibly reset the MCU when the chip temperature is too high.

The PB4 pin of CH32M030 supports ADC and OVP overvoltage reset, and the V_{HV} can be divided by 2 off-chip resistors and connected to the OVP of PB4. First, the real-time V_{HV} value can be obtained through ADC. The second is to set the overvoltage protection point of V_{HV} independently. When the voltage at the pin PB4 exceeds the OVP overvoltage reset threshold voltage (V_{OVP_REF}), the system will be placed in the reset state. For example, the upper resistor 200K and the lower resistor 15K will get an overvoltage reset voltage of about 21.5V. Refer to Table 3-4 for the value of V_{OVP_REF}.

1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are 2 modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.

1.4.6 Programmable Fast Interrupt Controller (PFIC)

The chip has a built-in Programmable Fast Interrupt Controller (PFIC) that supports up to 255 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. Currently the chip manages 5 core private interrupts and 31 peripheral interrupt management, with other interrupt sources reserved. the PFIC registers are all accessible in both user and machine privileged modes.

- Provide 5 non-maskable interrupt NMI
- Support 2-level interrupt nested entry and exit hardware automatic stack pressing and recovery without instruction overhead.
- Provide 4 programmable fast interrupt channels, and customize interrupt vector address.
- 31 peripheral interrupts, each interrupt request has independent trigger and mask bits and status bits.

1.4.7 Low-power Mode

The system supports 3 low-power modes, which can achieve the best balance under the conditions of low-power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in

working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Stop mode (STOP)

In this mode, the high frequency clock (HSE/HSI/PLL) domain is turned off, the contents of SRAM and register are maintained, and the state of I/O pin is maintained. After this mode wakes up, the system can continue to run. At this time, HSI is used as the default system clock source.

- Standby mode (STANDBY)

Set the PDDS and SLEEPDEEP bits, and execute the WFI/WFE instruction to enter. In this mode, the high frequency clock (HSE/HSI/PLL) domain is turned off, the contents of SRAM and register are maintained, and the state of I/O pin is maintained, which can achieve the lowest power consumption. After this mode wakes up, the system can continue to run. At this time, HSI is used as the default system clock source. The only difference between standby mode and stop mode is that in standby mode, the system voltage regulator will enter low power consumption mode.

Exit conditions: any external interrupt/event (EXTI signal) and external reset signal on RST, in which EXTI signal includes one of 36 external I/O ports (PA0~PA8, PA10~PA15, PB0~PB6, PB8~PB15, PC0~PC5), automatic wake-up signal, USB wake-up signal, USBPD wake-up signal, etc.

1.4.8 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 20 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can detect clock cycles with pulse widths less than the internal HB. The 36 general I/O ports can be connected to the corresponding 16 external interrupt sources.

1.4.9 General-purpose DMA Controller

A set of universal DMA controllers is built into the system, which manages seven channels, flexibly handles high-speed data transmission from memory to memory, from peripheral to memory and from memory to peripheral, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic, which supports the access request of one or more peripherals to the memory, and can configure the access priority, transmission length, source address and destination address of transmission, etc.

DMA for the main peripherals include: general / advanced timer TIMx, ADC, USART, I2C, SPI.

Note: DMA and CPU access the system SRAM after arbitration by the arbitrator.

1.4.10 Clock and Boot

The system clock source HSI is on by default. After no clock is configured or reset, the RC oscillator of the internal 8MHz is used as the default CPU clock, and then the external 4~25MHz clock or PLL clock can be selected. For low-power mode with clock off, the system will also automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

1.4.11 Analog-to-digital Converter (ADC)

CH32M030 has a built-in 12-bit ADC, supports up to 20 external channels, and has programmable channel sampling time, which can realize single, continuous, scanning or intermittent conversion. Providing analog watchdog function allows one or more selected channels to be monitored very accurately, which is used to monitor the channel signal voltage. When the monitored voltage exceeds the set threshold, it can be configured to generate a reset to protect the system.

Support external event trigger conversion, the trigger source includes the internal signal and external pin of the on-chip timer. Support DMA operation and ADC sliding average function.

ADC_IN9, ADC_IN10, ADC_IN18 and ADC_IN19 can be multiplexed into internal channels and connected to the output terminal of OPA. Please refer to Chapter 17.2 of CH32M030RM manual for register configuration.

1.4.12 Timer and Watchdog

Timers in the system include an advanced timer, a general timer, a reduced timer, a watchdog timer and a system time base timer.

- Advanced-control timer (TIM1)

The advanced-control timer is a 16-bit automatic load increment / decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer (TIM2)

The general-purpose timer is a 16-bit auto-load add / subtract counter with a programmable 16-bit prescaler and 4 independent channels, each of which supports input capture, output comparison, PWM generation and mono-pulse mode output. By alternate channels 3 and 4, channels 1 and 2 also have complementary PWM output with dead-time insertion.

- Streamlined timer (TIM3)

The streamlined timer is a 16-bit auto-loading up/down counter with a programmable 16-bit prescaler and two independent channels. Each independent channel supports input capture, output comparison, PWM generation and monopulse mode output, and also has simple dead-time control.

- Window watchdog (WWDG)

Window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- SysTick Timer (SysTick)

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions, which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, and can also be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.13 Universal Asynchronous Receiver Transmitter (UART)

CH32M030 provides a set of universal asynchronous transceivers (UART). It supports full-duplex asynchronous communication and half-duplex single-wire communication, and also supports LIN (Local Internet), which is compatible with IrDA SIR ENDEC transmission codec specification and modem (CTS/RTS hardware flow control) operation, and also allows multi-processor communication. It adopts fractional baud rate generator system and supports continuous communication of DMA operation.

1.4.14 I2C Bus

The chip provides an I2C bus interface, which can work in multi-host mode or slave mode, and complete all I2C bus specific timing, protocol, arbitration and so on. Both standard and fast communication speeds are supported.

The I2C interface provides 7-bit or 10-bit addressing and supports double-slave address addressing in 7-bit slave mode. Built-in hardware CRC generator / verifier.

1.4.15 Serial Peripheral Interface (SPI)

The chip provides a serial peripheral SPI interface, which supports master or slave operation and dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit choice, reliable communication hardware CRC generation/check, support DMA operation continuous communication.

1.4.16 Type-C and USB PD Controller

2 sets of USB Power Delivery controllers and PD transceiver PHY are built in, and four CC pins PA0/PA1/PA2/PA3 with high voltage resistance are provided. PA0 and PA1 are a pair of CC pins connected to a PD controller; PA2 and PA3 are a pair of CC pins connected to another PD controller. CC1/CC2/CC3/CC4 if there is a suffix r, it means that the controllable Rd pull-down resistor defined by the built-in Type-C specification is turned on by default.

Built-in multi-level pull-up current supports USB Type-C master-slave detection, automatic BMC coding and decoding and CRC, hardware edge control, power transmission control of USBPD2.0 and PD3.0, fast charging, UFP/PD Sink and DFP/PD power supply Source application, DRP application and dynamic switching, and can support PPS high-precision voltage regulation in cooperation with programmable charging current module ISINK.

1.4.17 Universal Serial Bus USB2.0 Full-speed Host/Device Controller (USBFS)

USB2.0 full-speed host controller and device controller (USBFS) follow USB2.0Fullspeed standard and support PDUSB. Provides 16 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronous/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up function. In addition, a 6-bit DAC, an output buffer and an output comparator are built in.

- Support USB Host and USB Device functions.

- Support USB 2.0 full-speed 12Mbps or low-speed 1.5Mbps.
- Support USB control transfer, batch transfer, interrupt transfer, synchronous/real-time transfer.
- Support up to 64-byte packets, built-in FIFO, interrupt and DMA.
- Support BC1.2 and DCP/CDP and other high voltage charging protocols
- Built-in 6-bit DAC and output buffer, support input comparison
- Supports programmable voltage output, programmable pull-up and pull-down resistors

1.4.18 OPA and CMP Characteristics

CH32M030 chip has 4 OPA operational amplifiers (OPA1, OPA2, OPA3, OPA4) and 3 CMP voltage comparators (CMP1, CMP2, CMP3), which support inductive positioning, ADC sampling non-inductive positioning, comparator non-inductive positioning, and single-resistance or double-resistance current sampling schemes.

OPA1 and OPA2 support self-biased programmable gain operational amplifier (PGA). Among them, the output result of OPA1 is connected to the voltage comparator CMP1 and ADC channel IN19; inside the chip; The output of OPA2 is connected to the voltage comparator CMP2 and ADC channel IN18 inside the chip.

OPA3 and OPA4 support single-ended and differential inputs, and PGA magnification can be selected by changing the configuration, and internal self-bias voltage is also provided. Among them, the output result of OPA3 is connected to the voltage comparator CMP2 or CMP3 and ADC channel IN9; inside the chip; The output of OPA4 is connected to the voltage comparator CMP3 and ADC channel IN10 inside the chip.

CMP1 supports optional hysteresis characteristics, digital filtering at the output, and optional output filtering.

CMP2 supports optional hysteresis, optional internal N-terminal bias and digital filtering at the output. Its P-side channel can be input by GPIO or connected with OPA in the chip. Its N-terminal channel can be input by GPIO or connected with DAC output inside the chip.

CMP3 supports optional hysteresis, optional internal N-terminal bias, and digital filtering at the output. Its P-side channel can be input by GPIO or connected with OPA in the chip. Its N-terminal channel is input by GPIO; The voltage comparison result OUT0 is analog output by GPIO, and OUT1 and OUT2 are push-pull output through GPIO port. In addition, inside the chip, the output channel of CMP3 is connected to the four channels of TIM2 to capture the trigger, and also connected to the BKIN channel of TIM1 as the brake source of TIM1 to realize over-current protection.

These OPA and CMP can be combined into 2 groups of AC small signal amplifiers and decoders (QII1 and QII2) and 2 groups of differential input current sampling (ISP1 and ISP2).

1.4.18.1 AC Small Signal Amplification Decoder (QII)

The chip supports 2 sets of AC small signal amplifiers and decoders QII1 and QII2. Among them, QII1 consists of an adjustable gain amplifier OPA1 at the front stage, a voltage comparator CMP1 at the rear stage and a digital filter; QII2 consists of a front-stage adjustable gain amplifier OPA2, a rear-stage multiplexed voltage comparator CMP2 and a digital filter.

The input AC small signal is amplified by OPA, shaped into digital signal by voltage comparator, filtered by digital filter and decoded, which can achieve high quality and low bit error rate in the transmission process. The amplified signal can also be sent to ADC for decoding.

- QII1 and QII2 output channels are directly connected to internal ADC channels or comparator CMP inputs.

- QII1 and QII2 support PGA self-biasing and multiple PGA gain options and digital filtering.
- The N-terminal of comparator CMP2 in QII2 supports an optional internal self-bias voltage.

1.4.18.2 Differential Input Current Sample (ISP)

CH32M030 supports 2 sets of differential input current sampling ISP1 and ISP2, and supports double resistance current sampling and overcurrent protection. ISP1 consists of an adjustable gain amplifier OPA3 at the front stage and a voltage comparator CMP2 or CMP3 multiplexed at the back stage; ISP2 consists of an adjustable gain amplifier OPA4 in the front stage and a voltage comparator CMP3 in the rear stage.

ISP1 and ISP2 support differential or single-ended applications. When applied differentially, ISP1 and ISN1/PA8 pins are a pair of differential inputs, and ISP2/PA10 and ISN2/PA11 pins are another pair of differential inputs; However, in single-ended application, there is no need to input ISN at the negative terminal. At this time, the ISN1/PA8 and ISN2/PA11 pins can be used for any purpose, such as ADC or GPIO.

ISP collects current through external resistor to get weak voltage signal, which is amplified by closed-loop amplifier OPA and sent to ADC or comparator.

- ISP1 and ISP2 support differential or single-ended inputs with configurable gain and output DC level.
- ISP1 and ISP2 output channels are directly connected to the ADC internal channels or comparator CMP inputs.

1.4.19 Programmable Current Sink Module ISINK/Source Current Module ISOURCE

The system provides 2 sets of programmable injection current modules ISINK and 2 sets of source current modules ISOURE.

ISINK, a programmable current injection module, supports 10-bit current precision, and can be used for high-precision voltage regulation of external DC-DC in 20mV steps to realize PPS protocol.

The source current module can be used for external low-cost NTC temperature-sensing resistor, etc., and the temperature can be calculated by ADC.

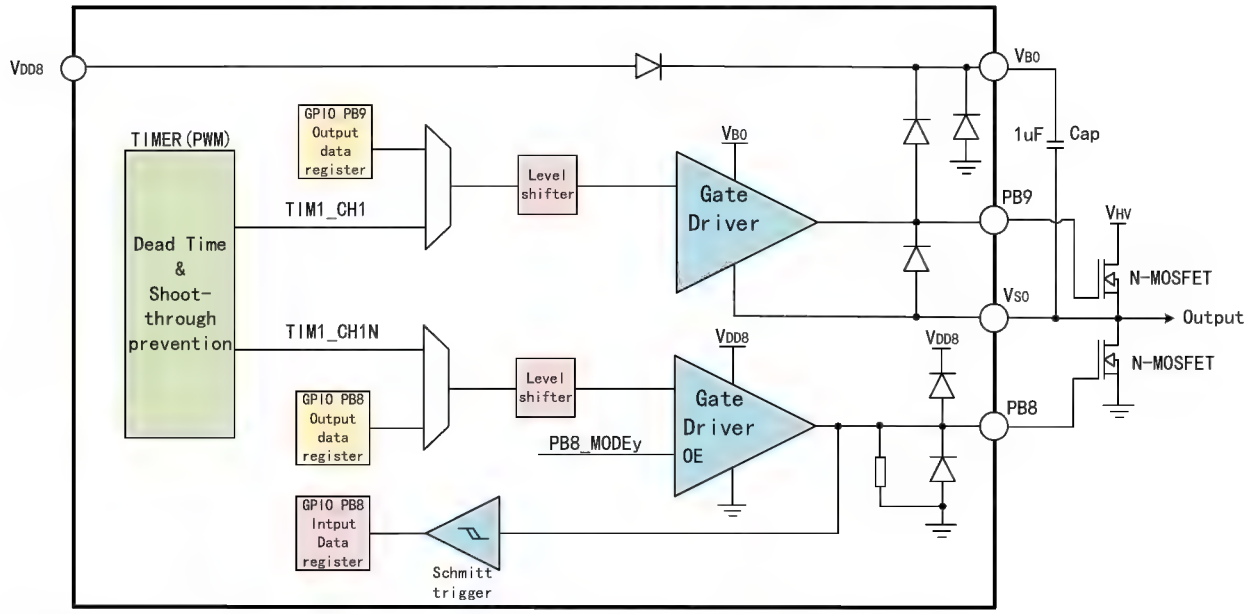
1.4.20 Gate Driver

CH32M030 integrates four independent half-bridge drivers, each half-bridge includes a low-voltage bootstrap diode, high-side and low-side level shift circuits, high-side and low-side output drive circuits, and supports four pairs of gate drives of N-type MOSFET power tubes. Only one capacitor is needed to store the bootstrap power supply externally, and the gate drive voltage depends on V_{DD8}, and it can be adjusted from 5V to 10V in 4 steps.

4 independent half-bridges can form a three-phase half-bridge, which is used to drive the grid of a three-phase motor and is controlled by PB8~PB13 signals generated by TIM1. Four independent half-bridges can also form two groups of full-bridges for 2 independent full-bridge drives, which are controlled by PB8~PB11 signals generated by TIM1 and PB12~PB15 signals generated by TIM2 respectively. The timer generates PWM signal, which supports dead-time control and over-current protection braking control.

Figure 1-4 below shows the structural block diagram of a single half-bridge driver.

Figure 1-4 Structural block diagram of single half-bridge driver



Note: Cap is off-chip capacitor; N-MOSFET is off-chip N-type MOSFET power tube.

1.4.21 General-purpose Input/Output Interface (GPIO)

The system provides 3 sets of GPIO ports with 37 GPIO pins (PA0~PA8, PA10~PA15, PB0~PB15, PC0~PC5). All GPIO pins can be configured as outputs (push-pull or open-drain) by software, and all GPIO pins except PB7, PB9, PB11, PB13 and PB15 can be configured as input or multiplexed peripheral functional ports. Most GPIO pins are shared with digital or analog multiplexing peripherals, providing a locking mechanism to freeze the IO configuration to avoid accidental writing to I/O registers.

PB8～PB15 are pre-driven MV I/O pins powered by V_{DD8}, PB7 is a high-voltage open-drain output pin, PC5 is a high-voltage HV I/O pin powered by V_{HV}, and the rest are ordinary I/O pins powered by V_{DD33}.

PB9, PB11, PB13 and PB15 are push-pull outputs, and the output is low by default, so input is not supported.

Except PB7～PB15 and PC5, all GPIO pins support controllable pull-ups, among which CC1/CC2/CC3/CC4 provide multistage pull-up current.

PB0 and PB1 have built-in pull-down resistors that can be turned on by default, adjusted and turned off, which are adjusted and controlled by two groups of PDE and DAC in EXTEN_CTLR1, and can provide pull-down current; CC1/CC2/CC3/CC4 if there is a suffix r, it means that the controllable Rd pull-down resistor defined by the built-in Type-C specification is turned on by default; PA0/CC1R and PA1/CC2R pins have built-in controllable Rd pull-down resistors, so it is recommended to turn off the pull-down when used as GPIO push-pull output. PB8, PB10, PB12 and PB14 have built-in pull-down resistors that cannot be turned off; None of the other GPIO pins have built-in pull-down resistors.

MV I/O pins (PB8~PB15) are powered by V_{DD8}. Changing the power supply of V_{DD8} will change the high value of MV pin output level to adapt to the external interface level. Among them, the power supply of PB9, PB11, PB13 and PB15 is bootstrapping power supply based on V_{DD8}, which is VB when high level is output and VS when low level is output. HV I/O pin PC5 is powered by V_{HV}, and the external interface level can be adapted by changing the high value of output level of HV I/O pin. The ordinary I/O pin is powered by V_{DD33}, and the external

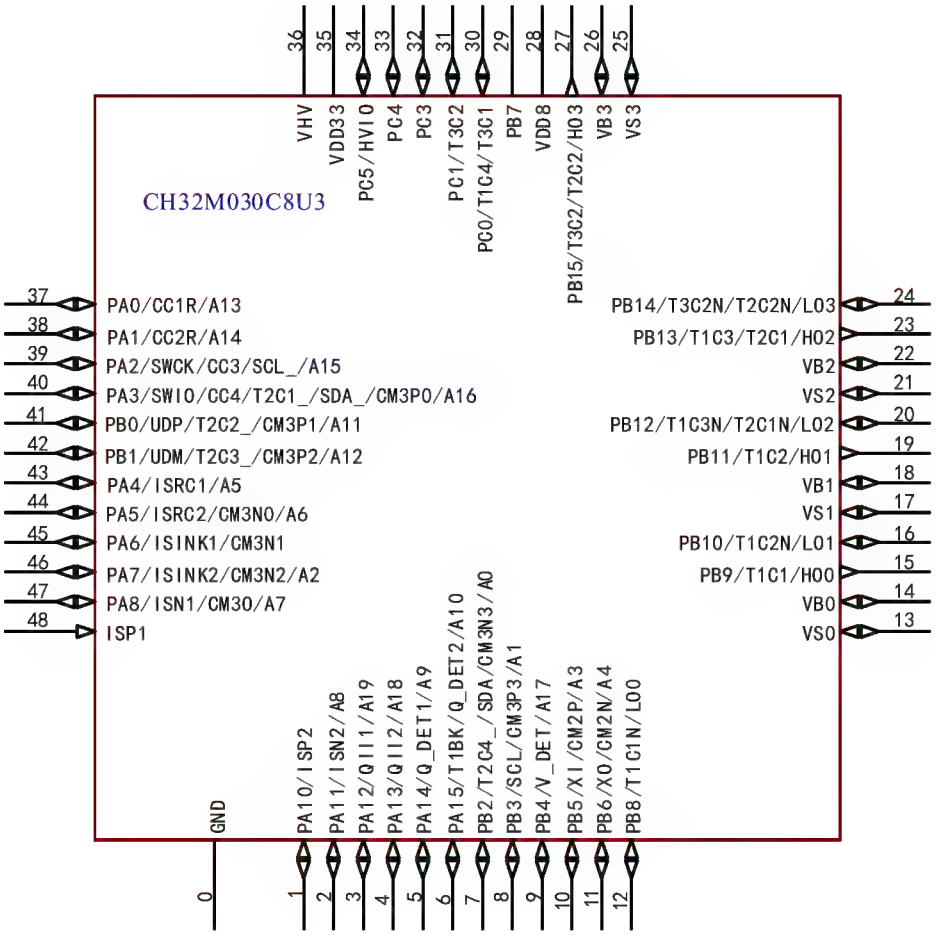
interface level can be adapted by changing the high value of the output level of the ordinary I/O pin. Please refer to Chapter 2 Pin Description for specific pins.

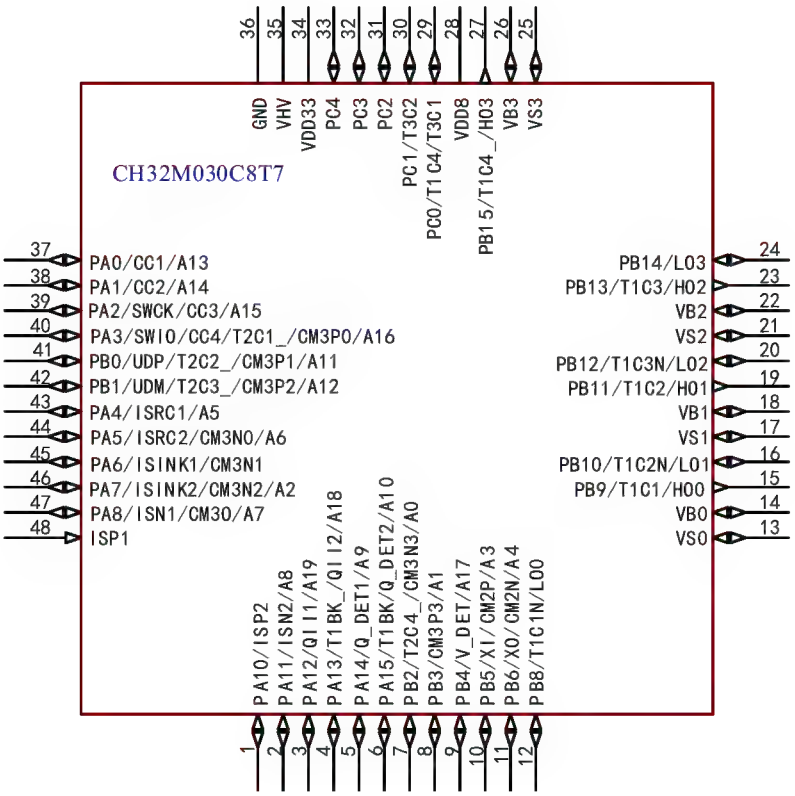
1.4.22 Serial Debug Interface (SDI)

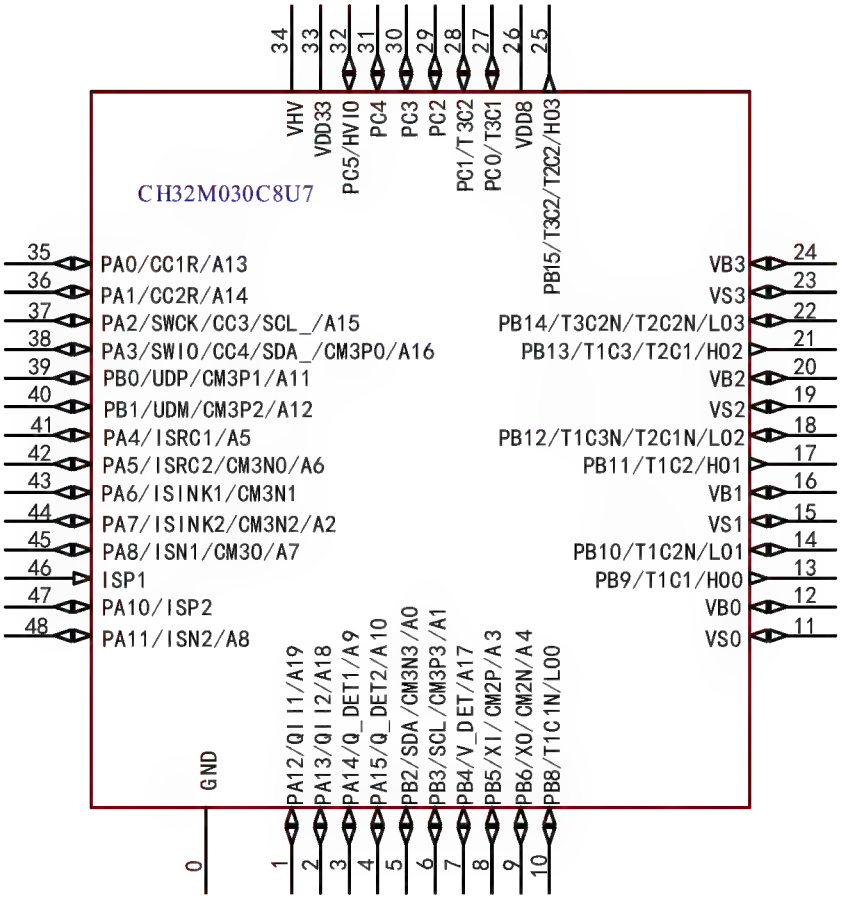
The core comes with 1-wire SDI Serial Debug Interface and 2-wire SDI Serial Debug Interface. The system supports 2 debugging modes: 1-wire SDI is the default debugging mode, which corresponds to SWIO pin (Single Wire Input Output), while 2-wire SDI corresponds to SWDIO and SWCLK pin, which can be used to increase the speed when applying to download. After the system is powered on or reset, the default debugging interface pin function is turned on, and the debugging pin multiplexing function can be turned off as needed after the main program runs.

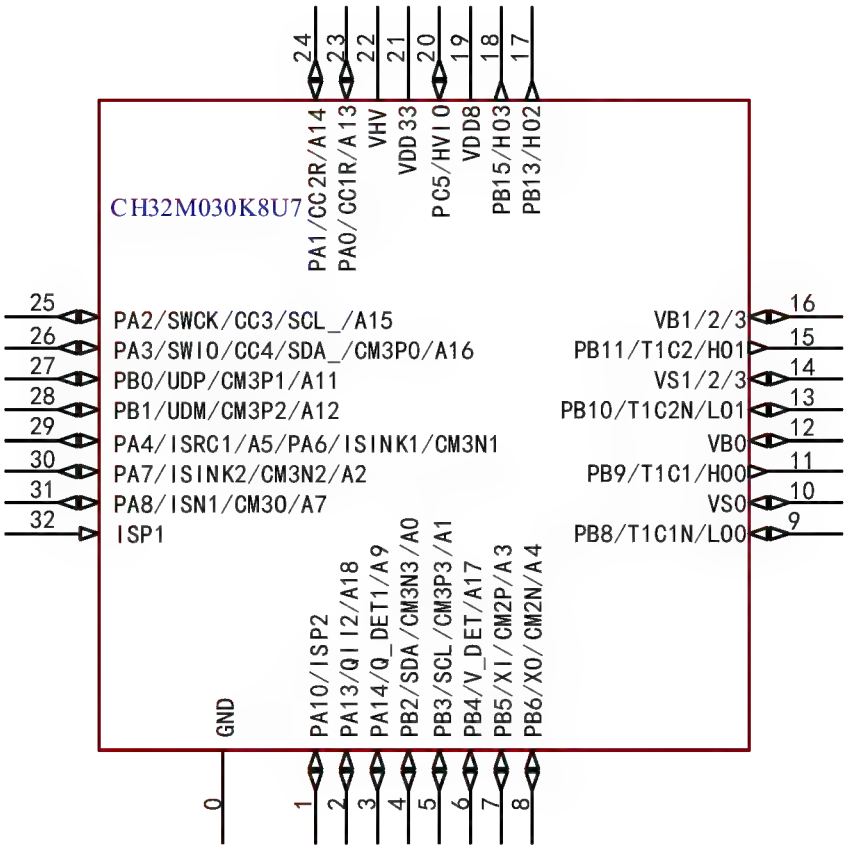
Chapter 2 Pinouts and Pin Definition

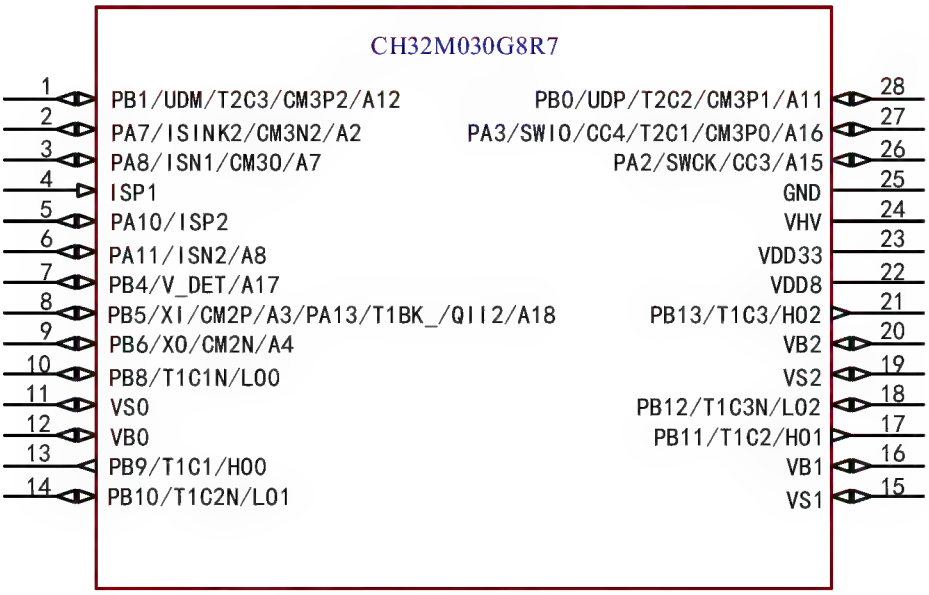
2.1 Pinouts




CH32M030C8T7
36 GND
35 VHV
34 VDD33
33 PC4
32 PC3
31 PC2
30 PC1/T3C2
29 PC0/T1C4/T3C1
28 VDD8
27 PB15/T1C4_/HO3
26 VB3
25 VS3
37 PA0/CC1/A13
38 PA1/CC2/A14
39 PA2/SWCK/CC3/A15
40 PA3/SWIO/CC4/T2C1_/CM3P0/A16
41 PB0/UDP/T2C2_/CM3P1/A11
42 PB1/UDM/T2C3_/CM3P2/A12
43 PA4/ISRC1/A5
44 PA5/ISRC2/CM3N0/A6
45 PA6/ISINK1/CM3N1
46 PA7/ISINK2/CM3N2/A2
47 PA8/ISN1/CM30/A7
48 ISP1
24 PB14/LO3
23 PB13/T1C3/HO2
22 VB2
21 VS2
20 PB12/T1C3N/LO2
19 PB11/T1C2/HO1
18 VB1
17 VS1
16 PB10/T1C2N/LO1
15 PB9/T1C1/HO0
14 VB0
13 VS0
1 PA10/ISP2
2 PA11/ISN2/A8
3 PA12/QII1/A19
4 PA13/T1BK_/QII2/A18
5 PA14/Q_DET1/A9
6 PA15/T1BK/Q_DET2/A10
7 PB2/T2C4_/CM3N3/A0
8 PB3/CM3P3/A1
9 PB4/V_DET/A17
10 PB5/XI/CM2P/A3
11 PB6/XO/CM2N/A4
12 PB8/T1C1N/LO0


CH32M030C8U7
34 VHV
33 VDD33
32 PC5/HVIO
31 PC4
30 PC3
29 PC2
28 PC1/T3C2
27 PC0/T3C1
26 VDD8
25 PB15/T3C2/T2C2/HO3
35 PA0/CC1R/A13
36 PA1/CC2R/A14
37 PA2/SWCK/CC3/SCL_/A15
38 PA3/SWIO/CC4/SDA_/CM3P0/A16
39 PB0/UDP/CM3P1/A11
40 PB1/UDM/CM3P2/A12
41 PA4/ISRC1/A5
42 PA5/ISRC2/CM3N0/A6
43 PA6/ISINK1/CM3N1
44 PA7/ISINK2/CM3N2/A2
45 PA8/ISN1/CM30/A7
46 ISP1
47 PA10/ISP2
48 PA11/ISN2/A8
24 VB3
23 VS3
22 PB14/T3C2N/T2C2N/LO3
21 PB13/T1C3/T2C1/HO2
20 VB2
19 VS2
18 PB12/T1C3N/T2C1N/LO2
17 PB11/T1C2/HO1
16 VB1
15 VS1
14 PB10/T1C2N/LO1
13 PB9/T1C1/HO0
12 VB0
11 VS0
0 GND
1 PA12/QII1/A19
2 PA13/QII2/A18
3 PA14/Q_DET1/A9
4 PA15/Q_DET2/A10
5 PB2/SDA/CM3N3/A0
6 PB3/SCL/CM3P3/A1
7 PB4/V_DET/A17
8 PB5/XI/CM2P/A3
9 PB6/XO/CM2N/A4
10 PB8/T1C1N/LO0





Note: The alternate functions in the pin diagram are abbreviated.

Example: A: ADC_(A13: ADC_IN13)

T: TIM_(T2C4:TIM2_CH4, T1C1N: TIM1_CH1N, T1BK:TIM1_BKIN)

CM3: CMP3_(CM3P2: CMP3_P2, CM3N2: CMP3_N2)

CM2: CMP2_(CM2P: CMP2_P, CM2N: CMP2_N)

SWCK: SWCLK

SWI0: SWDIO

ISRC: ISOURCE

2.2 Pin Definitions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-1 Pin definitions

Pin number					Pin name	Pin type (1)	I/O characteristic (1)(3)	Main function (after reset)	Default alternate function	Remapping function(2)
QSOP28	QFN32	QFN48	QFN48X7_A	LQFP48						
-	0	0	0	-	GND	P	-	GND		
5	1	47	1	1	PA10	I/O/A	-	PA10	ISP2	
6	-	48	2	2	PA11	I/O/A	-	PA11	ADC_IN8/ISN2	SPI_MOSI_2
-	-	1	3	3	PA12	I/O/A	-	PA12	ADC_IN19/QII1	
8	2	2	4	4	PA13(7)	I/O/A	-	PA13	ADC_IN18/QII2	TIM1_BKIN_1
-	3	3	5	5	PA14	I/O/A	-	PA14	ADC_IN9/ADC_ETR/ UART_CTS/Q_DET1	UART_CTS_1/I2C_SDA_2
-	-	4	6	6	PA15	I/O/A	-	PA15	ADC_IN10/TIM1_BKIN/UART_RTS/RST(4) /Q_DET2	TIM1_BKIN_2/TIM1_BKIN_3/ TIM1_BKIN_4/UART_RTS_1/ I2C_SCL_2
-	4	5	7	7	PB2	I/O/A	-	PB2	ADC_IN0/TIM3_CH1N/ I2C_SDA/CMP3_N3	TIM2_CH4_1/TIM2_CH4_3/ TIM2_CH2N_1/TIM2_CH2N_3/ TIM3_CH1_ETR_2/ TIM3_CH2_1/UART_CTS_3/ UART_CTS_4/UART_CTS_5
-	5	6	8	8	PB3	I/O/A	-	PB3	ADC_IN1/TIM3_CH2N/ I2C_SCL/CMP3_P3	TIM3_CH2_2/TIM3_CH2N_1/ UART_RTS_3/UART_RTS_4/ UART_RTS_5
7	6	7	9	9	PB4(11)	I/O/A	-	PB4	ADC_IN17/CMP3_OUT1/V_DET	TIM3_CH1N_2
8	7	8	10	10	PB5(7)	I/O/A	-	PB5	ADC_IN3/XI/ CMP3_OUT2/CMP2_P0	TIM3_CH2N_2/TIM3_CH2_3/ TIM2_CH1_ETR_3/ UART_RX_2/SPI_MOSI_1
9	8	9	11	11	PB6	I/O/A	-	PB6	ADC_IN4/XO/CMP2_N0	ADC_ETR_1/TIM2_CH2_3/ TIM3_CH2N_3/UART_TX_2/ I2C_SDA_1/SPI_SCK_1
10	9	10	12	12	PB8	I/O	MV/PD	PB8	LO0/TIM1_CH1N	TIM1_CH1N_1/TIM1_CH1N_2/ TIM1_CH1N_4
11	10	11	13	13	V_{SO}	P	-	V_{SO}		

12	12	12	14	14	V_{BO}	P	-	V_{BO}		
13	11	13	15	15	PB9	O	MVO	PB9	HO0/TIM1_CH1	TIM1_CH1_1/TIM1_CH1_2/ TIM1_CH1_4
14	13	14	16	16	PB10	I/O	MV/PD	PB10	LO1/TIM1_CH2N	TIM1_CH2N_1/TIM1_CH2N_2/ TIM1_CH2N_4
15	14	15	17	17	V_{S1}(8)	P	-	V_{S1}		
16	16	16	18	18	V_{B1}(9)	P	-	V_{B1}		
17	15	17	19	19	PB11	O	MVO	PB11	HO1/TIM1_CH2	TIM1_CH2_1/TIM1_CH2_2/ TIM1_CH2_4
18	-	18	20	20	PB12	I/O	MV/PD	PB12	LO2/TIM1_CH3N	TIM1_CH3N_1/TIM1_CH3N_4/ TIM2_CH3_2/TIM2_CH1N_2/ TIM3_CH1N_4
19	14	19	21	21	V_{S2}(8)	P	-	V_{S2}		
20	16	20	22	22	V_{B2}(9)	P	-	V_{B2}		
21	17	21	23	23	PB13	O	MVO	PB13	HO2/TIM1_CH3	TIM1_CH3_1/TIM1_CH3_4/ TIM2_CH1_ETR_2/ TIM3_CH1_ETR_4
-	-	22	24	24	PB14	I/O	MV/PD	PB14	LO3	TIM1_CH3N_2/TIM2_CH4_2/ TIM2_CH2N_2/TIM3_CH2N_4
-	14	23	25	25	V_{S3}(8)	P	-	V_{S3}		
-	16	24	26	26	V_{B3}(9)	P	-	V_{B3}		
-	18	25	27	27	PB15	O	MVO	PB15	HO3	TIM1_CH3_2/TIM1_CH4_1/ TIM2_CH2_2(10)/TIM3_CH2_4
22	19	26	28	28	V_{DD8}	P	-	V_{DD8}		
-	-	-	29	-	PB7	O	HVOD	PB7		
-	-	27	30	29	PC0	I/O	-	PC0	TIM1_CH4/RST(4) TIM3_CH1_ETR/ UART_RX	TIM1_CH3N_3/TIM1_CH3N_4/ TIM3_CH1_ETR_1
-	-	28	31	30	PC1	I/O	-	PC1	TIM1_ETR/TIM3_CH2/ UART_TX	TIM1_ETR_1/TIM1_CH2N_3/ TIM1_CH2N_4/TIM3_CH1N_1/ UART_TX_1
-	-	29	-	31	PC2	I/O	-	PC2		TIM1_CH4_2/TIM1_CH1N_3/ TIM1_CH1N_4/UART_RX_1
-	-	30	32	32	PC3	I/O	-	PC3	SPI_MOSI	TIM1_CH1_3/TIM1_CH1_4
-	-	31	33	33	PC4	I/O	-	PC4	SPI_MISO	TIM1_CH2_3/TIM1_CH2_4/ SPI_MISO_2
-	20	32	34	-	PC5	I/O	HV	PC5		TIM1_CH4_3/ TIM2_CH2_2(10)
23	21	33	35	34	V_{DD33}	P	-	V_{DD33}		
24	22	34	36	35	V_{HV}	P	-	V_{HV}		
25	-	-	-	36	GND	P	-	GND		

-	23	35	37	37	PA0[5]	I/O/A	-	PA0	ADC_IN13/CC1(CC1R) /SPI_NSS	TIM1_CH3_3/TIM1_CH3_4/ SPI_NSS_2
-	24	36	38	38	PA1[5]	I/O/A	-	PA1	ADC_IN14/CC2(CC2R) /SPI_SCK	TIM1_CH4_4/SPI_SCK_2/ SPI_SCK_3
26	25	37	39	39	PA2[5]	I/O/A	-	PA2	ADC_IN15/SWCLK/ CC3	TIM3_CH1_ETR_3/ UART_RX_4/UART_TX_5/ UART_CTS_2/I2C_SCL_1/ I2C_SCL_3/SPI_NSS_1/ SPI_NSS_3
27	26	38	40	40	PA3[5]	I/O/A	-	PA3	ADC_IN16/SWDIO/ SWIM/CC4/CMP3_P0	TIM2_CH1_ETR_1/ UART_RX_5/UART_TX_4/ I2C_SDA_3
28	27	39	41	41	PB0	I/O/A	-	PB0	ADC_IN11/UDP/ CMP3_P1	TIM2_CH2_1/UART_RX_3
1	28	40	42	42	PB1	I/O/A	-	PB1	ADC_IN12/UDM/ CMP3_P2	TIM2_CH3_1/TIM2_CH3_3/ TIM2_CH1N_1/TIM2_CH1N_3/ UART_TX_3
-	29	41	43	43	PA4[6]	I/O/A	-	PA4	ADC_IN5/TIM2_CH4 / TIM2_CH2N/ISOURCE1	TIM1_ETR_2/TIM1_ETR_3/ TIM1_ETR_4/TIM3_CH1N_3/ UART_RTS_2/SPI_MISO_1/ SPI_MISO_3
-	-	42	44	44	PA5	I/O/A	-	PA5	ADC_IN6/ TIM2_CH1_ETR/ CMP3_N0/ISOURCE2	
-	29	43	45	45	PA6[6]	I/O/A	-	PA6	TIM2_CH2/CMP3_N1/ ISINK1	
2	30	44	46	46	PA7	I/O/A	-	PA7	ADC_IN2/TIM2_CH3 / TIM2_CH1N/CMP3_N2/ ISINK2	
3	31	45	47	47	PA8	I/O/A	-	PA8	ADC_IN7/MCO/ CMP3_OUT0/ISN1	SPI_MOSI_3
4	32	46	48	48	ISP1	A	-	ISP1		

Note 1: Explanation of table abbreviations:

I = TTL/CMOS Schmitt input, supporting the input of V_{DD33} voltage range;

O = CMOS level three-state output, supporting the output of V_{DD33} voltage range;

P = Power supply.

MV= Pre-driving voltage pin, which supports the input and output of V_{DD8} voltage range;

MVO= Pre-driving voltage pin, which supports the output of V_{DD8} voltage range;

HV= High voltage pin, which supports input and output of V_{HV} voltage range;

HVOD= High voltage pin, supporting open-drain output in V_{HV} voltage range;

PD= Built-in pull-down resistor that cannot be turned off, which can be used to drive the gate of N-MOSFET;

A= Analog signal input or output, supporting V_{DD33} voltage range.

Note 2: The underlined value of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example, SPI_MOSI_2 indicates that the corresponding bit of AFIO register is configured as 10b.

Note 3: All GPIO pins support controllable pull-up except PB7~PB15 and PC5. PB0 and PB1 have built-in pull-down resistors that are turned on by default, adjustable and turned off, and can provide pull-down current; CC1/CC2/CC3/CC4 if there is a suffix R, it means that the controllable Rd pull-down resistor defined by the built-in Type-C specification is turned on by default; PA0/CC1R and PA1/CC2R pins are internally provided with controllable Rd pull-down resistors; PB8, PB10, PB12 and PB14 have built-in pull-down resistors that cannot be turned off; None of the other GPIO pins have built-in pull-down resistors.

Note 4: For the reset pin, its position selection is controlled by the user word configuration bit RST_PIN_SEL. When bit RST_PIN_SEL = 1, PA15 is the reset pin; When bit RST_PIN_SEL = 0, PC0 is the reset pin.

Note 5: When V_{HV} < 5V and PA0~PA3 are used as ADC input channels or GPIO push-pull outputs, the voltage range is about 0V ~ (V_{DD33}-1.7V).

Note 6: For CH32M030K8U7 chip, PA4 and PA6 pins are short-bonded inside the chip, and it is forbidden to configure both IO as output function.

Note 7: For CH32M030G8R7 chip, the pins PB5 and PA13 are short-circuited inside the chip, and it is forbidden to configure both IO as output functions.

Note 8: For CH32M030K8U7 chip, VS1, VS2 and VS3 pins are shorted inside the chip.

Note 9: For CH32M030K8U7 chip, VB1, VB2 and VB3 pins are shorted inside the chip.

Note 10: The PWM output of TIM2_CH2 is changed to PC5 pin output when bit[11:10] TIM2_RM of register AFIO_PCFR1 = 10 and bit[12] CH2_PWMOUT_EN of TIM2_CTLR1 = 1. PC5 is an open source output when it is used for TIM2_CH2 output, and if TIM2_CH2 is at high level, PC5 is at high level; If TIM2_CH2 is low, PC5 is high impedance state.

Note 11: When PB4 is used as a V_{HV} partial pressure monitoring function, the input voltage must not exceed V_{DD33}-0.9V.

Table 2-2 CH32M030 exclusive pin and function description

Name	Description
LO0,LO1,LO2,LO3	The output of the internal low-side gate driver supports the input and controls the gate of the N-type MOSFET.
HO0,HO1,HO2,HO3	The output of the internal high-side gate driver controls the gate of the N-type MOSFET.
V_{S0},V_{S1},V_{S2},V_{S3}	Floating ground of internal high-side gate driver.
V_{B0},V_{B1},V_{B2},V_{B3}	For the bootstrap power supply of the internal high-side gate driver, it is suggested to externally connect the capacitance of 1uF~10uF to their respective floating ground.

2.3 Pin Alternate Functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-3 Pin alternate and remapping functions

Alternate / Pin	ADC	TIM1	TIM2/3	UART	SYS	USB	I2C	SPI	ANA
PA0	ADC_IN13	TIM1_CH3_3 TIM1_CH3_4				CC1 (CC1R)		SPI_NSS SPI_NSS_2	
PA1	ADC_IN14	TIM1_CH4_4				CC2 (CC2R)		SPI_SCK SPI_SCK_2 SPI_SCK_3	
PA2	ADC_IN15		TIM3_CH1_ETR_3	UART_RX_4 UART_TX_5 UART_CTS_2	SWCLK	CC3	I2C_SCL_1 I2C_SCL_3	SPI_NSS_1 SPI_NSS_3	
PA3	ADC_IN16		TIM2_CH1_ETR_1	UART_RX_5 UART_TX_4	SWDIO SWIM	CC4	I2C_SDA_3		CMP3_P0
PA4	ADC_IN5	TIM1_ETR_2 TIM1_ETR_3 TIM1_ETR_4	TIM2_CH4 TIM2_CH2N TIM3_CH1N_3	UART_RTS_2				SPI_MISO_1 SPI_MISO_3	ISOURCE1
PA5	ADC_IN6		TIM2_CH1_ETR						CMP3_N0 ISOURCE2
PA6			TIM2_CH2						CMP3_N1 ISINK1
PA7	ADC_IN2		TIM2_CH3 TIM2_CH1N						CMP3_N2 ISINK2
PA8	ADC_IN7				MCO			SPI_MOSI_3	CMP3_OUT0 ISN1
PA10									ISP2
PA11	ADC_IN8							SPI_MOSI_2	ISN2
PA12	ADC_IN19								QII1
PA13	ADC_IN18	TIM1_BKIN_1							QII2
PA14	ADC_IN9 ADC_ETR			UART_CTS UART_CTS_1			I2C_SDA_2		Q_DET1
PA15	ADC_IN10	TIM1_BKIN TIM1_BKIN_2 TIM1_BKIN_3 TIM1_BKIN_4		UART_RTS UART_RTS_1	RST		I2C_SCL_2		Q_DET2
PB0	ADC_IN11		TIM2_CH2_1	UART_RX_3		UDP			CMP3_P1
PB1	ADC_IN12		TIM2_CH3_1 TIM2_CH3_3 TIM2_CH1N_1 TIM2_CH1N_3	UART_TX_3		UDM			CMP3_P2
PB2	ADC_IN0		TIM2_CH4_1 TIM2_CH4_3 TIM2_CH2N_1 TIM2_CH2N_3 TIM3_CH1_ETR_2 TIM3_CH2_1 TIM3_CH1N	UART_CTS_3 UART_CTS_4 UART_CTS_5			I2C_SDA		CMP3_N3
PB3	ADC_IN1		TIM3_CH2_2 TIM3_CH2N TIM3_CH2N_1	UART_RTS_3 UART_RTS_4 UART_RTS_5			I2C_SCL		CMP3_P3
PB4	ADC_IN17		TIM3_CH1N_2						CMP3_OUT1 V_DET
PB5	ADC_IN3		TIM3_CH2N_2 TIM3_CH2_3	UART_RX_2	XI			SPI_MOSI_1	CMP3_OUT2 CMP2_P0

Alternate Pin	ADC	TIM1	TIM2/3	UART	SYS	USB	I2C	SPI	ANA
			TIM2_CH1_ETR_3						
PB6	ADC_IN4 ADC_ETR_1		TIM2_CH2_3 TIM3_CH2N_3	UART_TX_2	XO		I2C_SDA_1	SPI_SCK_1	CMP2_N0
PB8		TIM1_CH1N TIM1_CH1N_1 TIM1_CH1N_2 TIM1_CH1N_4							
PB9		TIM1_CH1 TIM1_CH1_1 TIM1_CH1_2 TIM1_CH1_4							
PB10		TIM1_CH2N TIM1_CH2N_1 TIM1_CH2N_2 TIM1_CH2N_4							
PB11		TIM1_CH2 TIM1_CH2_1 TIM1_CH2_2 TIM1_CH2_4							
PB12		TIM1_CH3N TIM1_CH3N_1 TIM1_CH3N_4	TIM2_CH3_2 TIM2_CH1N_2 TIM3_CH1N_4						
PB13		TIM1_CH3 TIM1_CH3_1 TIM1_CH3_4	TIM2_CH1_ETR_2 TIM3_CH1_ETR_4						
PB14		TIM1_CH3N_2	TIM2_CH4_2 TIM2_CH2N_2 TIM3_CH2N_4						
PB15		TIM1_CH3_2 TIM1_CH4_1	TIM2_CH2_2 TIM3_CH2_4						
PC0		TIM1_CH4 TIM1_CH3N_3 TIM1_CH3N_4	TIM3_CH1_ETR TIM3_CH1_ETR_1	UART_RX	RST				
PC1		TIM1_ETR TIM1_ETR_1 TIM1_CH2N_3 TIM1_CH2N_4	TIM3_CH2 TIM3_CH1N_1	UART_TX UART_TX_1					
PC2		TIM1_CH4_2 TIM1_CH1N_3 TIM1_CH1N_4		UART_RX_1					
PC3		TIM1_CH1_3 TIM1_CH1_4						SPI_MOSI	
PC4		TIM1_CH2_3 TIM1_CH2_4						SPI_MISO SPI_MISO_2	
PC5		TIM1_CH4_3	TIM2_CH2_2						

Chapter 3 Electrical Characteristics

3.1 Test Condition

Unless otherwise specified and marked, all voltages are based on GND.

All minimum and maximum values will be guaranteed under the worst environmental temperature, power supply voltage and clock frequency conditions. Typical values can be used for design guidance based on one of the following three environments:

1. Single V_{HV} power supply, room temperature 25℃, V_{HV} = 12V;
2. External direct power supply for V_{DD8}, room temperature 25℃, V_{HV} = 12V, V_{DD8} = 8V, at this time, $V_{DD8} \leq V_{HV}$; is required;
3. External direct power supply for V_{DD33} and V_{DD8}, room temperature 25℃, V_{HV} = 12V, V_{DD8} = 8V, V_{DD33} = 3.3V, at this time, $V_{DD33} \leq V_{DD8} \leq V_{HV}$ is required.

The data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested in the production line. On the basis of comprehensive evaluation, the minimum and maximum values are obtained by statistics after sample testing. Unless otherwise specified as measured values, the characteristic parameters shall be guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1-1 Typical circuit for conventional power supply (Single V_{HV} power supply)

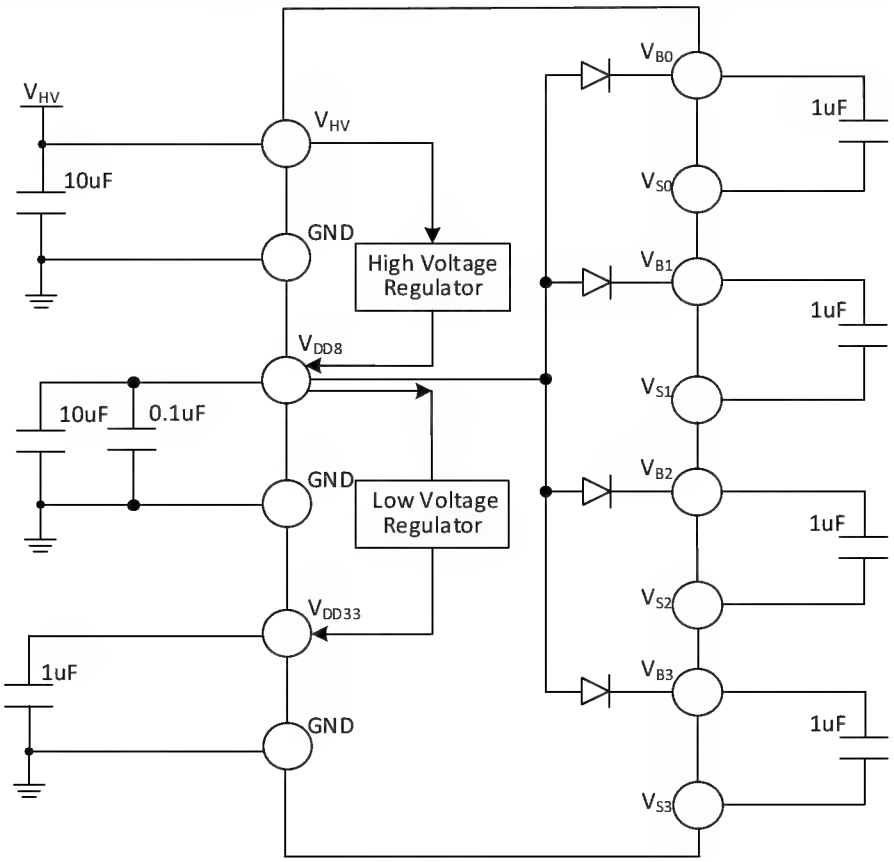


Figure 3-1-2 Typical circuit for conventional power supply (Single V_{DD8} power supply)

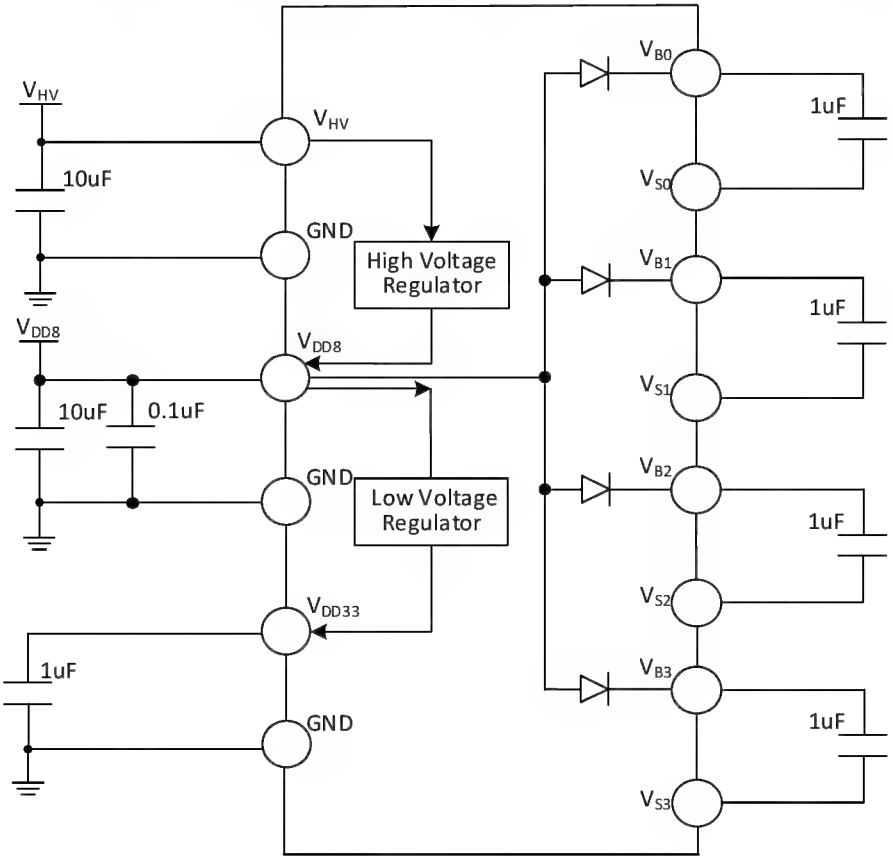
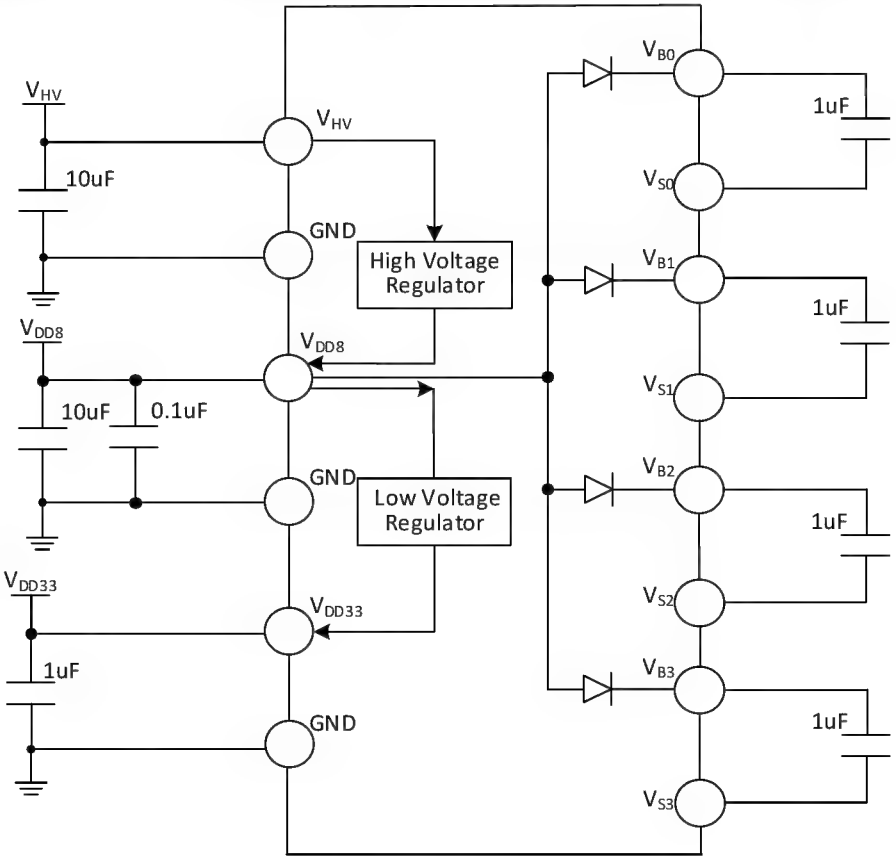


Figure 3-1-3 Typical circuit with conventional power supply (External direct power supply for V_{DD33} and V_{DD8})



3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description		Min.	Max.	Unit
T_A	Ambient temperature at work	CH32M030C8T7, CH32M030C8U7 CH32M030G8R7, CH32M030K8U7	-40	105	℃
		CH32M030C8U3	-40	125	℃
T_S	Ambient temperature during storage		-40	150	℃
V_{HV}-GND	External main supply voltage (V_{HV})		-0.3	30	V
V_{DD8}-GND	Supply voltage of internal low voltage regulator and MV I/0 pin (V_{DD8})		-0.3	12	V
V_{DD33}-GND	Power supply voltage of common I/O pin and analog part (V_{DD33})		-0.3	3.8	V
V_{IN}	Input voltage on HV high voltage I/O pin PC5		-0.3	V_{HV}+7	V
	Voltage on HV high voltage I/O pin PB7		-0.3	40	V
	Input voltage on high-voltage I/O pin CCx (there may be leakage)		-0.3	28	V

	Input voltage on common I/O pin	-0.3	V_{DD33}+0.3	V
V_B	High-side bootstrap supply voltage	-0.3	40	V
V_{BPEAK}	High-side bootstrap 1% duty cycle pulse voltage	-0.3	42	V
V_S	High side floating ground voltage	-2	30	V
V_{SPEAK}	High-side suspended 1% duty cycle pulse voltage	-5	32	V
$V_{B\ S}$	Voltage difference between high-side bootstrap power supply and floating ground	-0.3	12	V
V_{HO}	Output voltage of high-side driver	V_S-0.3	V_B+0.3	V
V_{LO}	Output voltage of low-side driver	-0.3	V_{DD8}+0.3	V
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage to external pins USB and PD (HBM)	4K		V
	ESD electrostatic discharge voltage (HBM) to external pins USB and PD.	2K		V
I_{PEAKVB}	V_B built-in diode 1% duty cycle pulse output current		70	mA
I_{AVVB}	V_B built-in diode continuous output current		7	mA
I_{VHV}	Continuous input current (supply current) for all V_{HV} pins.		60	mA
I_{GND}	Total current (outflow current) of all GND common ground pins		200	mA
I_{IO}	Sink current or source current on HV high-voltage I/O pins		+/-5	mA
	Sink current or source current on MV pre-drive I/O pins		+/-80	mA
	Sink current or source current on other common I/O pins		+/-30	mA
$I_{INJ(PIN)}$	XI pin of HSE		+/-4	mA
	Sink current on other pins		+/-4	mA
$\sum I_{INJ(PIN)}$	Total injection current of all IO and control pins		+/-20	mA

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK}	Internal HB clock frequency	T_A = -40°C~105°C		72	MHz
		T_A = -40°C~125°C		68	MHz
V_{HV}	Supply voltage of internal high-voltage regulator and HV I/O pins	T_A = -40°C~105°C	4.0	29.0	V
		T_A = -40°C~125°C	4.3	28.0	V
V_{DD8}	Supply voltage of internal low-voltage regulator and MVI/0 pin	T_A = -40°C~105°C	4.0	10.5	V
		T_A = -40°C~125°C	4.3	10.0	V
V_{DD33}	Power supply voltage of common I/O pin and analog part		3.1	3.5	V
V_S	High side floating ground voltage	T_A = -40°C~105°C	-2.0	29.0	V
		T_A = -40°C~125°C	-2.0	28.0	V

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0.1	∞	us/V
	V_{DD} fall time rate		40	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$	Power-on/power-off reset threshold	V_{DD33} rising edge threshold	2.8	3.0	3.1	V
		V_{DD33} falling edge threshold	2.6	2.9	3.0	V
		V_{DD8} threshold	3.05	3.15	3.25	V
$V_{PDRhyst}$	PDR hysteresis	V_{DD33} threshold		100	150	mV
V_{OVP_REF}(3)	OVP overvoltage reset threshold voltage	Rising edge		1.5		V
		Falling edge		1.45		V
V_{DD8}	Output voltage of high voltage regulator	VDD8_SEL[1:0] = 00 and $V_{HV} \geq 5.8V$	4.9	5.0	5.1	V
		VDD8_SEL[1:0] = 01 and $V_{HV} \geq 8.8V$	7.8	8.0	8.2	V
I_{VDD8}	Load current of high voltage regulator (including all loads such as MVI/O and low voltage regulator)				35	mA
V_{DD33}	Output voltage of low voltage regulator		3.24	3.3	3.36	V
I_{VDD33}	Load current of low-voltage regulator (including all loads such as common I/O and core regulator)				20	mA
T_{OTP}	Temperature point of OTP over-temperature protection	Heating process	130	145	160	℃
	Temperature point of removing over-temperature protection	Cooling process	125	135	150	℃
t_{RST}	Power-on reset delay			3 (2)		ms
	Other reset delay			300		us

Note: 1. Normal temperature test value.

2. The user configuration bit RST_MODE can increase the power-on reset delay.

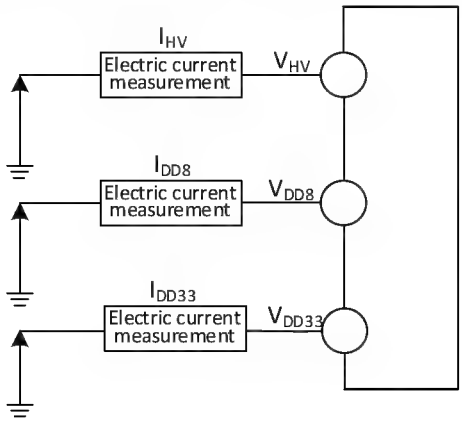
3.V_{OVP_REF} needs to determine the overvoltage protection point of V_{HV} voltage in combination with the ratio of off-chip resistor voltage division. For example, the upper resistor 200K and the lower resistor 15K will get an overvoltage reset voltage of about 21.5V.

3.3.3 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and

factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

Under the condition of room temperature V_{HV}=12V (V_{DD8}=8V, V_{DD33}=3.3V), during the test, I/O ports supporting pull-up input are configured in pull-up input mode, while others are configured in analog input mode. HSE=8M, HSI=8M (calibrated). Enable or turn off the power consumption of all peripheral clocks.

Table 3-5 Typical current consumption in Run mode, data processing code runs from the internal Flash

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{HV}	Supply current in Run mode	Running in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency.	F_{HCLK} = 72MHz	12.0	6.3	mA
			F_{HCLK} = 48MHz	9.0	4.9	
			F_{HCLK} = 24MHz	5.9	3.5	
			F_{HCLK} = 8MHz	1.9	1.4	
			F_{HCLK} = 4MHz	1.4	1.1	
		Running on high-speed external clock (HSE), HB pre-frequency division is used to reduce the frequency.	F_{HCLK} = 72MHz	12.2	6.5	mA
			F_{HCLK} = 48MHz	9.2	5.1	
			F_{HCLK} = 24MHz	6.1	3.7	
			F_{HCLK} = 8MHz	2.1	1.6	
			F_{HCLK} = 4MHz	1.6	1.3	

Note: The above are measured parameters.

Table 3-6 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM

Symbol	Parameter	Condition	Typ.	Unit

				All peripherals enabled	All peripherals disabled	
I_{HV}	Supply current in SLEEP mode (peripheral power supply and clock holding at this time)	Running in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency.	F_{HCLK} = 72MHz	9.5	3.9	mA
			F_{HCLK} = 48MHz	7.1	3.1	
			F_{HCLK} = 24MHz	4.7	2.3	
			F_{HCLK} = 8MHz	1.1	0.6	
			F_{HCLK} = 4MHz	0.7	0.5	
		Running on high-speed external clock (HSE), HB pre-frequency division is used to reduce the frequency.	F_{HCLK} = 72MHz	9.9	4.2	mA
			F_{HCLK} = 48MHz	7.5	3.4	
			F_{HCLK} = 24MHz	5.0	2.6	
			F_{HCLK} = 8MHz	1.4	0.9	
			F_{HCLK} = 4MHz	1.0	0.8	

Note: The above are measured parameters.

Table 3-7 Typical current consumption in Standby mode

Symbol	Parameter	Condition		Typ.	Unit
I_{HV}	Supply current in STOP mode	V_{HV} = 12V, V_{DD8} = 5V		104	uA
		V_{HV} = 12V, V_{DD8} = 8V		114	
		V_{HV} = 12V, V_{DD8} = 9V		123	
		V_{HV} = 12V, V_{DD8} = 10V		133	
	Supply current in STANDBY mode	V_{HV} = 12V, V_{DD8} = 5V	LSI on	76	uA
			LSI off	74	
		V_{HV} = 12V, V_{DD8} = 8V	LSI on	94	
			LSI off	92	
		V_{HV} = 12V, V_{DD8} = 9V	LSI on	102	
			LSI off	102	
		V_{HV} = 12V V_{DD8} = 10V	LSI on	114	
			LSI off	114	

Note: The above are measured parameters.

3.3.4 External Clock Source Characteristics

Table 3-8 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		4	8	25	MHz

V_{HSEH}(1)	XI input pin high voltage		0.8*V_{DD33}		V_{DD33}	V
V_{HSEL}(1)	XI input pin low voltage		0		0.2*V_{DD33}	V
$C_{in(HSE)}$	XI input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle		40	50	60	%
I_L	XI input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

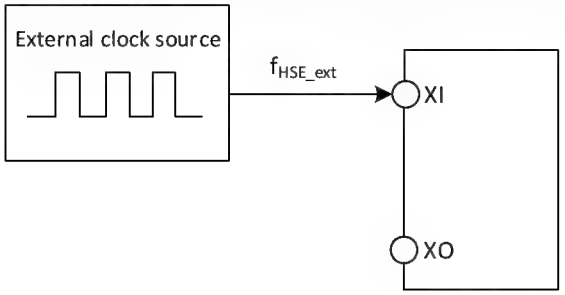


Table 3-9 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{XI}	Resonator frequency		4	8	25	MHz
R_F	Feedback resistor (no external)			250		kΩ
C_{LOAD}	Suggested load capacitance and corresponding crystal serial impedance R_S	R_S = 60Ω(1)		20		pF
I_2	HSE drive current	V_{DD33} = 3.3V, 20p load		0.3		mA
g_m	Transconductance of oscillator	Startup		16		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable		2(2)		ms

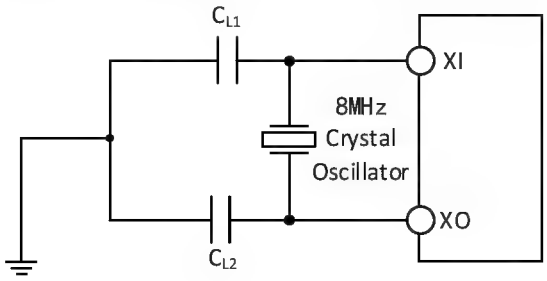
Note: 1. 25M crystal ESR is recommended not more than 80Ω, less than 25m can be appropriately relaxed.

2. Startup time refers to the time difference between when HSEON is turned on and when HSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally C_{L1} = C_{L2}.

Figure 3-4 Typical circuit of external 8M crystal



3.3.5 Internal Clock Source Characteristics

Table 3-10 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			8		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	T_A = 0℃~70℃	-1.5		1.5	%
		T_A = -40℃~85℃	-2.0		2.0	%
		T_A = -40℃~125℃	-2.2		2.2	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time			10		us
$I_{DD(HSI)}$	HSI oscillator power consumption		120	180	270	uA

Table 3-11 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		240	340	450	kHz
$DuTy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time			80		us
$I_{DD(LSI)}$	LSI oscillator power consumption			2		uA

3.3.6 Wakeup Time from Low-power Mode

Table 3-12 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	Wake up with HSI RC clock	24	us
t_{WUSTOP}	Wakeup from Stop mode	Wake up with HSI RC clock	255	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake-up	260	us

Note: The above are measured parameters.

3.3.7 Memory Characteristics

Table 3-13 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (128 bytes) program time		3.9	4.5	5.1	ms
t_{erase_page}	Page (128 bytes) erase time		3.9	4.5	5.1	ms
t_{ME}	Whole erase time		3.9	4.5	5.1	ms

Table 3-14 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase times	T_A = 25℃	10K	50K(1)		time

		T_A = 125℃	1K	5K(1)		time
t_{RET}	Data retention period		10			year

Note: 1. Actual number of operational erasures, not guaranteed.

3.3.8 I/O Port Characteristics

Table 3-15 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
V_{IH}	Standard I/O pin, input high level voltage	V_{DD33} = 3.3V	1.8		V_{DD33}	V
V_{IL}	Standard I/O pin, input low-level voltage	V_{DD33} = 3.3V	0		0.8	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD33} = 3.3V		300		mV
I_{lkg}	Input leakage current			0	+/-3	uA
R_{PU}	Pull-up equivalent resistance		30	45	60	kΩ
C_{IO}	I/O pin capacitance			5		pF

Table 3-16 General-purpose I/O pin output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{SINK}	Sink current of pin output low-level	V_{DD33} = 3.3V, pin voltage = 0.4V	14	20	27	mA
I_{SOURCE}	Source current of pin output high-level	V_{DD33} = 3.3V, pin voltage = V_{DD33}-0.4V	13	18	24	mA

Table 3-17 General-purpose I/O pin output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low, single pin sinks 8mA current.	$V_{DD33} \geq 3V$		0.5	V
V_{OH}	Output high, single pin outputs 8mA current.	$V_{DD33} \geq 3V$	V_{DD33}-0.5		V

Note: 1. When V_{HV} < 5V and PA0~PA3 output high level, the voltage can't reach the full width of V_{DD33}, which is about V_{DD33}-1.7V.

2. In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum rating given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground pin is relatively large, resulting in a voltage drop that makes the internal I/O voltage not reach the power supply voltage in the table, resulting in the driving current being less than the nominal value.

Table 3-18 Input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{max(IO)out}$	I/O pin output highest frequency	CL = 50pF, $V_{DD33} \geq 3V$		30	MHz
$t_{f(IO)out}$	Falling time of output high to low level	CL = 50pF, $V_{DD33} \geq 3V$		12	ns

$t_{r(IO)out}$	Rising time of output low to high level			12	ns
t_{EXTIpw}	EXTI controller detects the pulse width of external signal.		12		ns

3.3.9 MV I/O Pin Characteristics

Table 3-19 MV I/O pin static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD8}	Supply voltage		4.0	8.0	10.5	V
V_{IH}	I/O pin input high-level voltage		2.0		V_{DD8}	V
V_{IL}	I/O pin input low-level voltage		0		0.7	V
V_{hys}	Schmitt trigger hysteresis voltage			500		mV
I_{lkg}	I/O pin input leakage current	Pin voltage = GND	-5	0	5	uA
		Pin voltage = 5V	30	42	63	uA
R_{PD}	Pull-down equivalent resistance		80	120	170	kΩ
C_{IO}	I/O pin capacitance			10		pF

Table 3-20 MV I/O pin output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{LSINK}	Sink current of pin output low-level	V_{DD8} = 8V, pin voltage = 0.5V	75	110	145	mA
	Short-circuit current of pin output low-level	V_{DD8} = 8V, pin voltage = V_{DD8}		620		mA
	Sink current of pin output low-level	V_{DD8} = 5V, pin voltage = 0.5V	60	90	120	mA
	Short-circuit current of pin output low-level	V_{DD8} = 5V, pin voltage = V_{DD8}		320		mA
	Sink current of pin output low-level	V_{DD8} = 10V, pin voltage = 0.5V	80	120	160	mA
	Short-circuit current of pin output low-level	V_{DD8} = 10V, pin voltage = V_{DD8}		740		mA
$I_{LSOURCE}$	Source current of pin output high-level	V_{DD8} = 8V, pin voltage = V_{DD8}-0.5V	30	50	65	mA
	Short-circuit of pin output high-level	V_{DD8} = 8V, pin voltage = GND		350		mA
	Source current of pin output high-level	V_{DD8} = 5V, pin voltage = V_{DD8}-0.5V	25	38	55	mA
	Short-circuit of pin output high-level	V_{DD8} = 5V, pin voltage = GND		170		mA
	Source current of pin output high-level	V_{DD8} = 10V, pin voltage = V_{DD8}-0.5V	35	55	75	mA
	Short-circuit of pin output high-level	V_{DD8} = 10V, pin voltage = GND		480		mA

Note: 1. For the HO pin, the high level corresponds to V_B voltage and the low level corresponds to V_S voltage. The test condition is based on the difference V_{B_S} voltage, and the V_{B_S} voltage condition refers to the above-mentioned value of V_{DD8}.

2. When testing pin current and driver short-circuit current, it is suggested to adopt low duty cycle pulse test and consider the timely heat dissipation of the chip.

Table 3-21 MV I/O pin output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{LOL}	Output low, and a single pin sinks 50mA current.	$5V \le V_{DD8} \le 10V$		0.5	V
V_{LOH}	Output high, and a single pin outputs 25mA source current	$5V \le V_{DD8} \le 10V$	V_{DD8}-0.5		V

Note: If multiple I/O pins are driven at the same time under the above conditions, the total current cannot exceed the absolute maximum rating given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground pin is relatively large, resulting in a voltage drop that makes the internal I/O voltage not reach the power supply voltage in the table, resulting in the driving current being less than the nominal value.

Table 3-22 MV I/O pin input/output AC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$F_{Lmax(IO)out}$	I/O pin output highest frequency	CL = 2000pF, $5V \le V_{DD8} \le 10V$			400	kHz
$t_{Lf(IO)out}$	Falling time of output high to low	CL = 2000pF, $5V \le V_{DD8} \le 10V$		35	70	ns
$t_{Lr(IO)out}$	Rising time of output low to high			50	100	ns
$t_{LEXTIpw}$	EXTI controller detects the pulse width of external signal.		12			ns

3.3.10 HV I/O Pin Characteristics

Table 3-23 HV I/O pin static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HV}	Supply voltage		4.0		29.0	V
V_{HPC5}	Pin tolerant voltage when PC5 does not output.			V_{HV}	V_{HV}+6	V
V_{HPB7}	Pin tolerant voltage when PB7 does not output.			V_{HV}	38	V
V_{HIH}	I/O pin input high-level voltage		2.0		V_{HV}	V
V_{HIL}	I/O pin input low-level voltage		0		0.7	V
V_{Hhys}	Schmitt trigger voltage hysteresis			500		mV
I_{Hlkg}	I/O pin input leakage current		-5	0	5	uA
C_{HIO}	I/O pin capacitance			8		pF

Table 3-24 HV I/O pin output drive current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{HSINK}	Sink current of pin output low-level	V_{HV} = 29V, pin voltage = 0.5V	0.8	1.2	1.6	mA
	Short-circuit current of pin output low-level	V_{HV} = 29V, pin voltage = V_{HV}		5		mA
	Sink current of pin output low-level	V_{HV} = 8V, pin voltage = 0.5V	0.8	1.2	1.6	mA
	Short-circuit current of pin output low-level	V_{HV} = 8V, pin voltage = V_{HV}		5		mA
$I_{HSOURCE}$	Source current of pin output high-level	V_{HV} = 29V, pin voltage = V_{HV}-0.5V	0.5	0.9	1.3	mA
	Short-circuit of pin output high-level	V_{HV} = 29V, pin voltage = 0		8		mA
	Source current of pin output high-level	V_{HV} = 8V, pin voltage = V_{HV}-0.5V	0.5	0.9	1.3	mA
	Short-circuit of pin output high-level	V_{HV} = 8V, pin voltage = 0		8		mA

Note: When testing pin current and driver short-circuit current, it is recommended to adopt low duty cycle pulse test and consider the timely heat dissipation of the chip.

Table 3-25 HV I/O pin output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{HOL}	Output low, and a single pin sinks 2mA current.	5V ≤ V_{HV} ≤ 12V		0.5	V
V_{HOH}	Output high, and a single pin outputs 0.2mA source current	5V ≤ V_{HV} ≤ 12V	V_{HV}-0.5		V

Note: If multiple I/O pins are driven at the same time under the above conditions, the total current cannot exceed the absolute maximum rating given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground pin is relatively large, resulting in a voltage drop that makes the internal I/O voltage not reach the power supply voltage in the table, resulting in the driving current being less than the nominal value.

Table 3-26 HV I/O pin input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{Hmax(IO)out}$	I/O pin output highest frequency	CL = 20pF, 4V ≤ V_{HV} ≤ 29V		100	kHz
$t_{Hf(IO)out}$	Falling time of output high to low	CL = 20pF, 4V ≤ V_{HV} ≤ 29V		100	ns
$t_{Hr(IO)out}$	Rising time of output low to high			100	ns
$t_{HEXTIpw}$	EXTI controller detects the pulse width of external signal.		12		ns

3.3.11 USB/BC Interface UDP and UDM Characteristics

Table 3-27 USB/BC interface I/O pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	USB operating voltage		3.1	3.3	3.5	V
V_{SE}	Single ended receiver threshold	Rated voltage	1.2		1.9	V
R_{PU}	BC pin pull-up equivalent resistance	DAC = 100000	20	31	45	kΩ
R_{PD}	BC pin pull-down equivalent resistance	DAC = 100000	20	31	45	kΩ
I_{PU2}	BC pin weak pull-up current	PCS = 10, BC output voltage is 0.6V	7	10	15	uA
I_{PD3}	BC pin weak pull-down current	PCS = 11, BC output voltage is 0.6V	1	2	5	uA
I_{PD1}	BC pin pull-down current	PCS = 01, BC output voltage is 0.6V	55	80	120	uA
ET	DAC total error	V_{DD33} = 3.3V		0.3	1	LSB
V_{DACmax}	DAC maximum output voltage	V_{DD33} = 3.3V, uninhibited load	3.2	3.25		V
V_{DACmin}	DAC minimum output voltage	V_{DD33} = 3.3V, uninhibited load		0	0.02	V
R_{DAC}	DAC output impedance	V_{DD33} = 3.3V, turn off DAC buffer	12	15.5	20	kΩ
		V_{DD33} = 3.3V, turn on DAC buffer, $0.1V \le V_{DACB_OUT}^{(1)} \le V_{DD33}-0.1V$		17	25	Ω
I_{DDDAC}	DAC buffer supply current			135		uA
$V_{DACBmax}$	Maximum output voltage of DAC with buffer	V_{DD33} = 3.3V, load 10kΩ pull-down	3.1	3.2		V
$V_{DACBmin}$	Minimum output voltage of DAC with buffer	V_{DD33} = 3.3V, load 10kΩ pull-down		0.005	0.02	V
		V_{DD33} = 3.3V, load 10kΩ pull-up		0.08	0.15	V
tBuf	DAC buffer as the output delay of comparator			400	800	ns

Note: V_{DACB_OUT} is the output voltage of DAC with buffer.

3.3.12 USB PD Interface Characteristics

Table 3-28-1 PD interface I/O pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
tRise	Rising time	Time between 10% and 90% amplitude, no load.	300	430	600	ns
tFall	Falling time	Time between 10% and 90% amplitude, no load.	300	430	600	ns
vSwing	Output voltage swing (peak-to-peak)		1.00	1.12	1.20	V

zDriver	Output impedance	V_{DD33} = 3.3V, PD interface output 1.12V	26		90	Ω
		V_{DD33} = 3.3V, PD interface output 3.3V		40		Ω

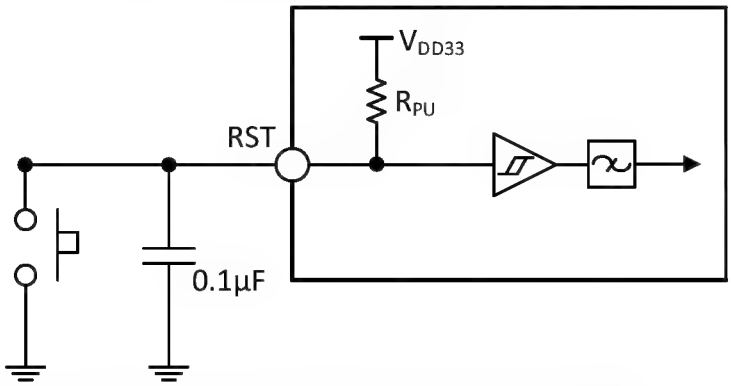
Table 3-28-2 Type-C interface I/O pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CCIH}	CC pin input high-level voltage	V_{DD33} = 3.3V, USBPDx_CC_HVT = 1 (x=0,1)	2.1		V_{DD33}	V
V_{CCIL}	CC pin input low-level voltage	V_{DD33} = 3.3V, USBPDx_CC_HVT = 1 (x=0,1)	0		1.9	V
V_{CChys}	Schmitt trigger voltage hysteresis	V_{DD33} = 3.3V, USBPDx_CC_HVT = 1 (x=0,1)		200		mV
I_{PUCC}	CC pin pull-up current	CCx_PU = 11 (x=1,2), PAD < V_{DD33}-0.6V	68	80	92	uA
		CCx_PU = 10 (x=1,2), PAD < V_{DD33}-0.6V	150	180	210	uA
		CCx_PU = 01 (x=1,2), PAD < V_{DD33}-0.6V	280	330	380	uA
Rd	CC pin built-in Rd pull-down resistor (for CCxR with R suffix)	CCx_PD = 1 (x=1,2), V_{DD33} ≥ 3.1V or external pull-up 330uA	4.08	5.1	6.12	kΩ
R_{wpd}	CC pin built-in weak pull-down resistor	CCx_PD = 0 (x=1,2)	250	600		kΩ
V_{AINCC}	CC pin ADC conversion voltage range	V_{HV} > 5V	0		V_{DD33}	V
		V_{HV} < 5V	0		V_{DD33}-1.7	V

3.3.13 RST Pin Characteristics

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin



Note: The capacitance in the figure is optional and can be used to filter out key jitter.

Table 3-29 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(RST)}$	RST input low-level voltage	V_{DD33} = 3.3V	0		0.8	V
$V_{IH(RST)}$	RST input high-level voltage	V_{DD33} = 3.3V	1.8		V_{DD33}	V
$V_{hys(RST)}$	RST Schmitt trigger voltage hysteresis		200			mV
R_{PU}	Pull up equivalent resistance		30	45	60	kΩ
$V_{F(RST)}$	RST input can be filtered pulse width.				60	ns
$V_{NF(RST)}$	RST input cannot filter pulse width.		230			ns

3.3.14 TIM Timer Characteristics

Table 3-30 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8		ns
F_{EXT}	Timer external clock frequency from CH1 to CH3		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	MHz
R_{esTIM}	Timer resolution			16	Bit
$t_{COUNTER}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1363	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		1363	us

3.3.15 I2C Interface Characteristics

Figure 3-6 I2C bus timing diagram

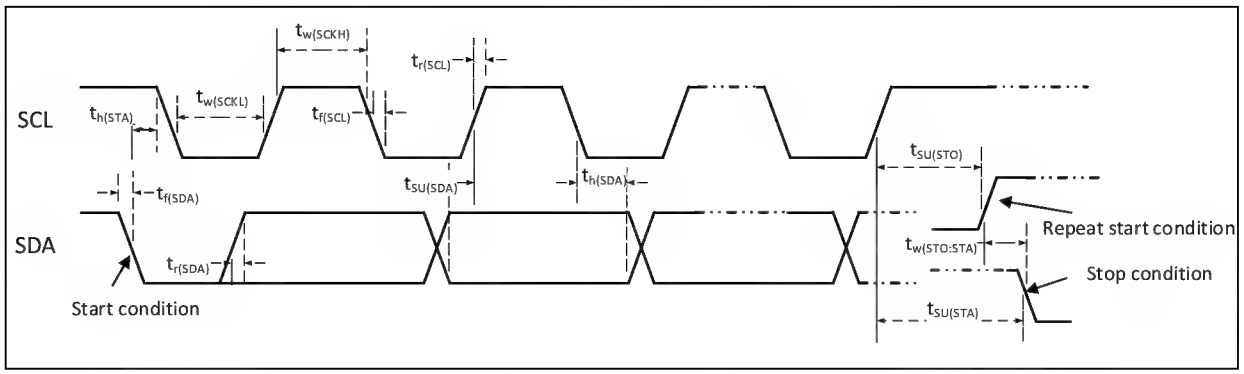


Table 3-31 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low-level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high-level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.16 SPI Interface Characteristics

Figure 3-7 SPI timing diagram in Master mode

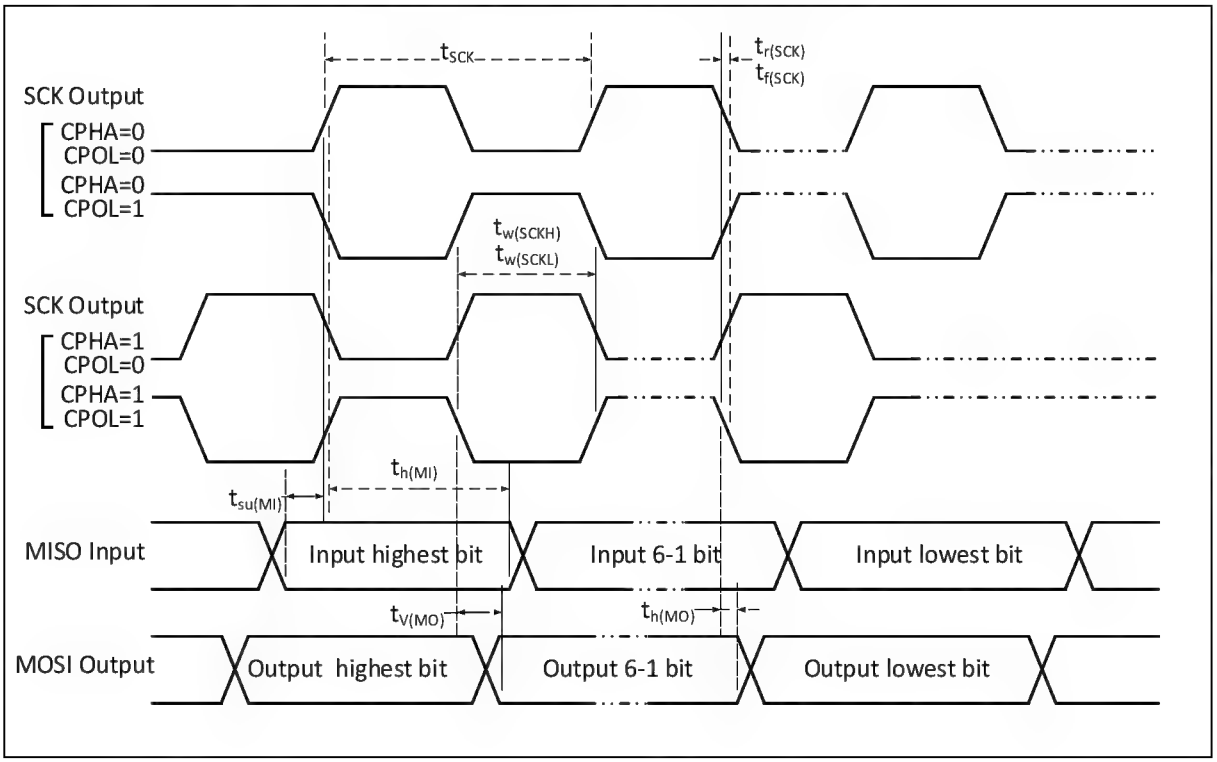


Figure 3-8 SPI timing diagram in Slave mode (CPHA = 0)

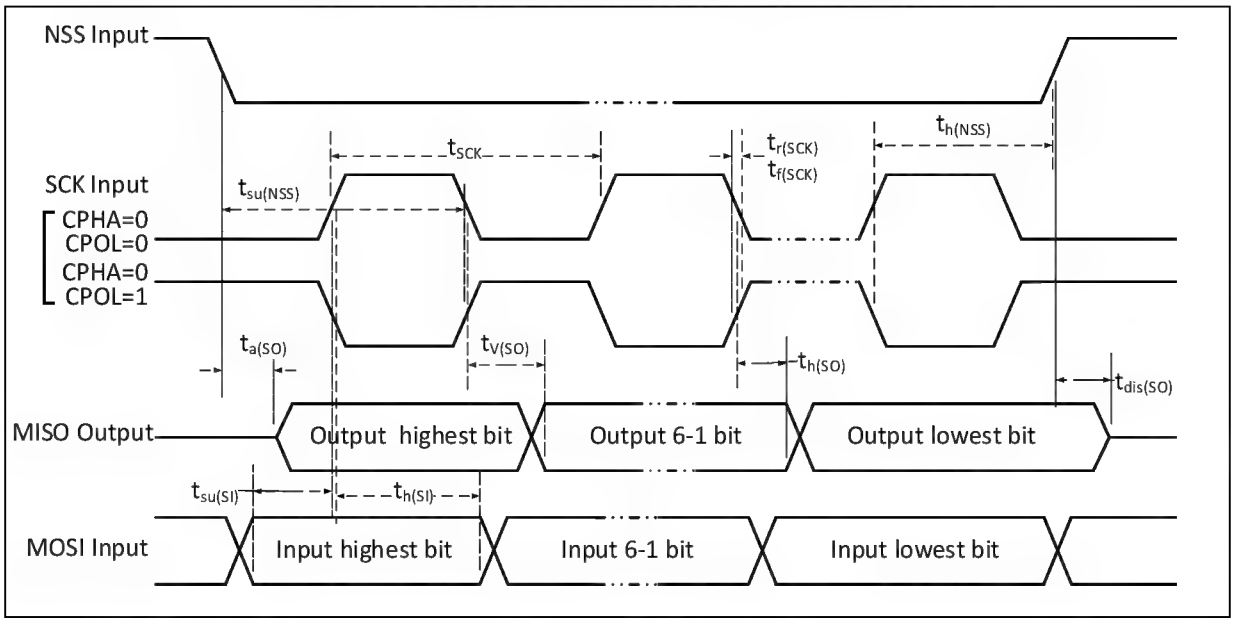


Figure 3-9 SPI timing diagram in Slave mode (CPHA = 1)

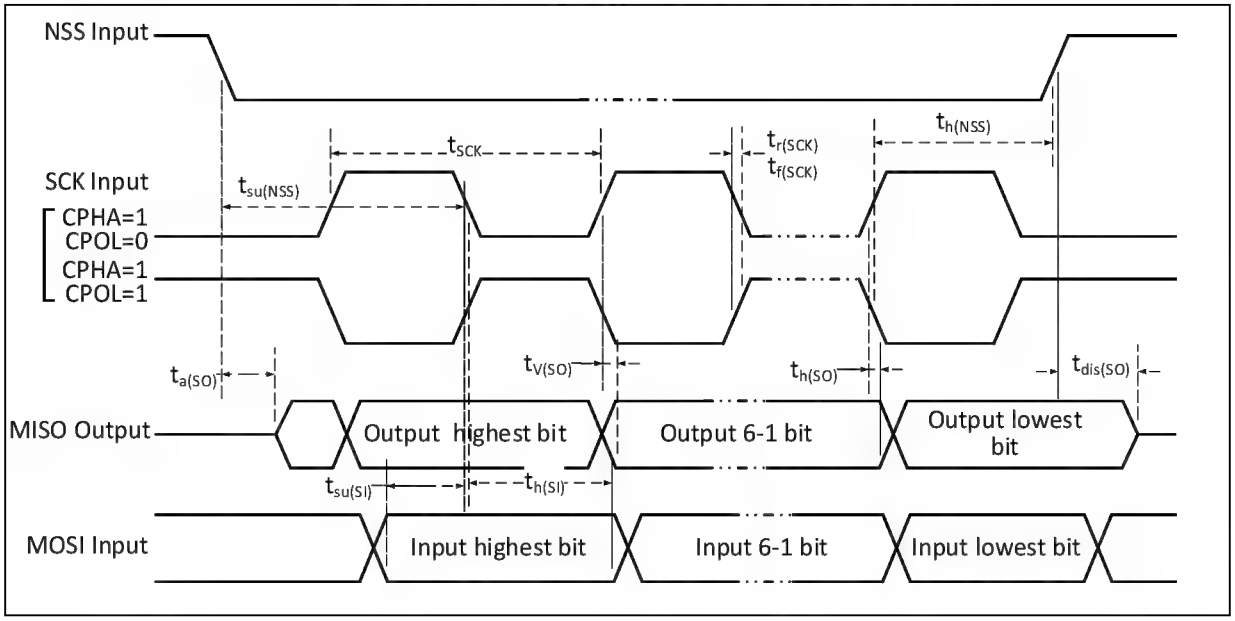


Table 3-32 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		36	MHz
		Slave mode		36	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2*t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{HCLK} = 24MHz, Prescaler factor = 4	70	97	ns

$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	12		ns
			HSRXEN = 1	12-0.5*t_{SCK}		
$t_{SU(SI)}$		Slave mode		4		ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	-4		ns
			HSRXEN = 1	0.5*t_{SCK}-4		
$t_{h(SI)}$		Slave mode		4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{HCLK} = 20MHz		0	1*t_{HCLK}	ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			15	ns
$t_{V(MO)}$		Master mode (After enable edge)			5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)		8		ns
$t_{h(MO)}$		Master mode (After enable edge)		0		ns

3.3.17 Analog/Digital Converter ADC Characteristics

Table 3-33 12-bit ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
I_{DDADC}	Supply current			1		mA
f_{ADC}	ADC clock frequency				18	MHz
V_{AIN}	Conversion voltage range		0		V_{DD33}	V
C_{ADC}	Internal sample and hold capacitance			6		pF
f_s	Sampling speed	f_{ADC} = 18MHz	250		1000	kHz
			1/72		1/18	f_{ADC}
t_s	Sampling time	f_{ADC} = 18MHz	0.31		3.31	us
			5.5		59.5	$1/f_{ADC}$
t_{STAB}	Power-on time			7		us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 18MHz	1		4	us
			18		72	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N = 12 (represents a 12-bit resolution).

Table 3-34 Maximum R_{AIN} when f_{ADC} = 18MHz

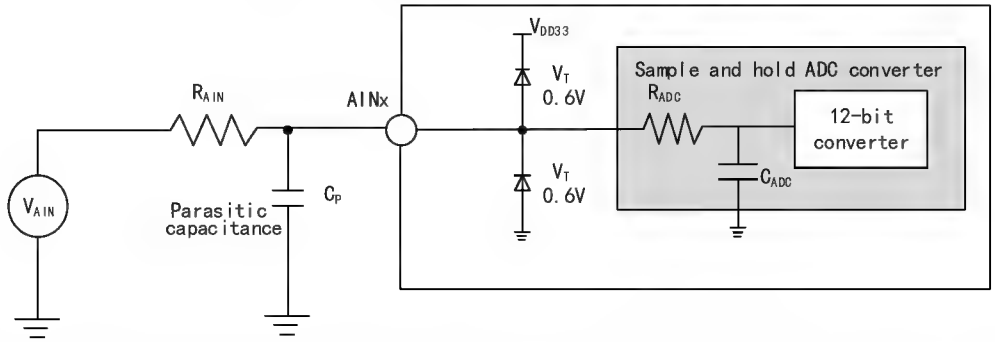
T_S(Cycle)	t_S(us)	Max. R_{AIN}(kΩ)
5.5	0.31	3.8
11.5	0.64	9.4
23.5	1.31	21
59.5	3.31	55

Table 3-35 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ET	Data total error	f_{ADC} = 18MHz, R_{AIN} < 4kΩ, V_{DD33} = 3.3V		±3	±8	LSB
EO	Offset error			±1	±3	
EG	Gain error			±2	±4	
ED	Differential nonlinear error			±3	±7	
EL	Integral nonlinear error			±3	±7	

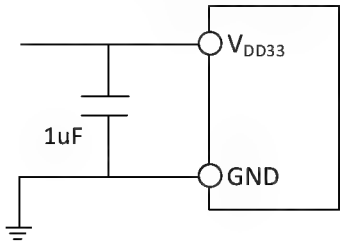
Note: Above parameters are guaranteed by design.

Figure 3-10 ADC typical connection diagram



C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-11 Analog power supply and decoupling circuit reference



3.3.18 OPA Characteristics

Table 3-36-1 OPA1 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

V_{DD33}	Supply voltage		3.1	3.3	3.5	V
I_{DDQII}	Supply current			270		uA
V_{CMIR}	Common-mode input voltage				V_{DD33}-1.5	V
$V_{IOFFSET}$	Input offset voltage			2	6	mV
Av(1)	Open loop gain			90		dB
BW(1)	OPA1 operational amplifier bandwidth	VO∈(0.3V, V_{DD33}-0.3V)		600		kHz
		VO∈(0.2V, V_{DD33}-0.2V)		500		
		VO∈(0.1V, V_{DD33}-0.1V)		400		
PGA_{GAIN}(1)	PGA gain error	Gain = 20	-1		1	%
		Gain = 40	-1		1	
R_{BIAS}	Bias resistance in QII1 mode			90		kΩ

Note: 1. Design parameters are guaranteed.

Table 3-36-2 OPA2 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
I_{DDQII}	Supply current			270		uA
V_{CMIR}	Common-mode input voltage				V_{DD33}-1.5	V
$V_{IOFFSET}$	Input offset voltage			2	6	mV
Av(1)	Open loop gain			90		dB
BW (1)	OPA2 operational amplifier bandwidth	VO∈(0.3V,V_{DD33}-0.3V)		600		kHz
		VO∈(0.2V,V_{DD33}-0.2V)		500		
		VO∈(0.1V,V_{DD33}-0.1V)		400		
PGA_{GAIN}(1)	PGA gain error	Gain = 5	-1		1	%
		Gain = 10	-1		1	
		Gain = 20	-1		1	
		Gain = 40	-1		1	
R_{BIAS}	Bias resistance in QII2 mode			90		kΩ

Note: 1. Design parameters are guaranteed.

Table 3-36-3 OPA3 and OPA4 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
I_{DDISP}	Supply current			420		uA
V_{CMIR}	Common-mode input voltage				V_{DD33}-1.5	V
$V_{IOFFSET}$	Input offset voltage			3	8	mV
Av(1)	Open loop gain			110		dB
G_{BW}(1)	Unity gain bandwidth			20		MHz
P_M(1)	Phase margin			75		°
PGA_{GAIN}(1)	Internal noninverting PGA gain error	Gain = 4	-1.3		1.3	%
		Gain = 8	-1.3		1.3	
		Gain = 16	-1.3		1.3	

		Gain = 55	-1.6		1.6	
	Differential input PGA gain error (differential input connected in series with 100Ω resistor)	Gain = 4	-1.3		1.3	%
		Gain = 8	-1.3		1.3	
		Gain = 16	-1.3		1.3	
		Gain = 55	-1.6		1.6	
	Differential input PGA gain error (differential input directly connected to low resistance signal source)	Gain = 4	-0.3		2.3	%
		Gain = 8	-0.3		2.3	
		Gain = 16	-0.3		2.3	
		Gain = 55	-0.6		2.6	
S_R(1)	Swing rate		10	20	30	V/us
V_{OHSAT}(1)	High saturation voltage	Non-loaded	V_{DD33}-300			mV
V_{OLSAT}(1)	Low saturation voltage	Non-loaded			300	mV
t_{WAKEUP}(1)	Off-to-wake time, 0.1%				1	us
eN(1)	Output noise density	1kHz		200		nV/ sqrt(Hz)
		10kHz		80		

Note: 1. Design parameters are guaranteed.

3.3.19 OPA Characteristics

Table 3-37-1 CMP1 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Power supply		3.1	3.3	3.5	V
V_{CMIR}	Common-mode input voltage			1.2	V_{DD33}-1.5	V
$V_{IOFFSET}$ (1)	Input offset voltage			3.5		mV
$I_{DDOPAMP}$	Consumption current			35		uA
V_{hys}	Hysteresis voltage	QII1_HYPSEL = 0		100		mV
		QII1_HYPSEL = 1		200		mV
t_D(1)	Comparator delay, V_{INP} varies from (V_{INN}-10mV) to (V_{INN}+10mV).	V_{INN} = 1.2V		40		ns

Note: 1. Design parameters are guaranteed.

Table 3-37-2 CMP2 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
V_{CMIR}	Common-mode input voltage		0		V_{DD33}	V
$V_{IOFFSET}$ (1)	Input offset voltage	Common mode input, 0.6V < V_{CMIR} <V_{DD33}-0.6V		2	6	mV
		Common mode input, V_{CMIR} < 0.6V or V_{CMIR} > V_{DD33}-0.6V		3.5	11	

$I_{DDOPAMP}$	Consumption current			55		uA
V_{hys}	Hysteresis voltage	QII2_HYPSEL[2:0] = 000		0		mV
		QII2_HYPSEL[2:0] = 001		5		
		QII2_HYPSEL[2:0] = 010		10		
		QII2_HYPSEL[2:0] = 011		20		
		QII2_HYPSEL[2:0] = 100		40		
		QII2_HYPSEL[2:0] = 101		50		
		QII2_HYPSEL[2:0] = 110		60		
		QII2_HYPSEL[2:0] = 111		120		
t_D(1)	Comparator delay, V_{INP} varies from (V_{INN}-100mV) to (V_{INN}+100mV).	V_{INN} = 1.2V		30		ns
DAC_{INL}	CMP2 internal DAC integration nonlinear error, 0.1V≤DAC_OUT≤3.1V, step = 200mV	V_{DD33} = 3.3V			30	mV

Note: 1. Design parameters are guaranteed.

Table 3-37-3 CMP3 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
V_{CMIR}	Common-mode input voltage		0		V_{DD33}	V
$V_{IOFFSET}$ (1)	Input offset voltage	Common mode input, 0.6V < V_{CMIR} < V_{DD33}-0.6V		2	6	mV
		Common mode input, V_{CMIR} < 0.6V or V_{CMIR} > V_{DD33}-0.6V		3.5	11	
$I_{DDOPAMP}$	Consumption current			50		uA
V_{hys}	Hysteresis voltage	HYS[1:0] = 00		0		mV
		HYS[1:0] = 01		10		mV
		HYS[1:0] = 10		20		mV
		HYS[1:0] = 11		40		mV
t_D(1)	Comparator delay, V_{INP} varies from (V_{INN}-100mV) to (V_{INN}+100mV).	0 ≤ V_{INN} ≤ V_{DD33}		17	50	ns
DACINL	CMP2 internal DAC integration nonlinear error, 0.1V≤DAC_OUT≤3.1V,	V_{DD33} = 3.3V			50	mV

	step = 200mV					

Note: 1. Design parameters are guaranteed.

3.3.20 ISINK Module Current Characteristics

Table 3-38 10-bit ISINK module current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
I_{STEP}(2)	Unit current value (1*LSB)			0.244		uA
I_{SW}	Current output range	V_{PAD} > 0.6V	0		1023*LSB	uA
I_{ISO} (1)	Current absolute value error		-2*LSB		2*LSB	uA
I_{INL} (1)	current integration nonlinear error of	After calibration			±4	LSB
I_{DNL} (1)	Current differential nonlinear error				±2	LSB
I_{TC} (1)	ISINK current temperature characteristics	T_A = 0~55℃, Input 0x200	-3		+2	LSB
		T_A = -40~105℃, Input 0x200	-6		+5	LSB
$t_{SETTLING}$(1)	Settling time (full range: the input code changes from the minimum value to the maximum value, and ISNK_OUT reaches 1 * LSB of its final value)			1	3	us
v_{UPDATE}(1)	When the input code changes slightly (from numerical value I to i+1*LSB), the maximum frequency of correct ISNK_OUT is obtained.				1	MS/s
t_{WAKEUP}(1)	Time to wake up from off state			2	4	us

Note: 1. Design parameters are guaranteed.

3.3.21 ISOURCE Module Current Characteristics

Table 3-39 ISOURCE module current characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33}	Supply voltage		3.1	3.3	3.5	V
I_{SW} (1)	Current output range	ISRCx_SEL = 0 (x = 1, 2), V_{PAD} < V_{DD33}-0.6V	6	8	10	uA
		ISRCx_SEL = 1 (x = 1, 2), V_{PAD} < V_{DD33}-0.6V	26	32	38	uA
I_{TC} (1)	ISOURCE current temperature characteristics	T_A = -40~105℃	-2		+2	%

Note: 1. Design parameters are guaranteed.

Chapter 4 Package and Ordering Information

Packages

Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN48X7_A	7*7mm	0.5mm	19.7mil	Quad Flat No-lead Package	CH32M030C8U3
LQFP48	7*7mm	0.5mm	19.7mil	Low-profile Quad Flat Package	CH32M030C8T7
QFN48	5*5mm	0.35mm	13.8mil	Quad Flat No-lead Package	CH32M030C8U7
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32M030K8U7
QSOP28	3.9*9.9mm	0.635mm	25.0mil	Quarter-sized Outline Package	CH32M030G8R7

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 4-1 LQFP48 package

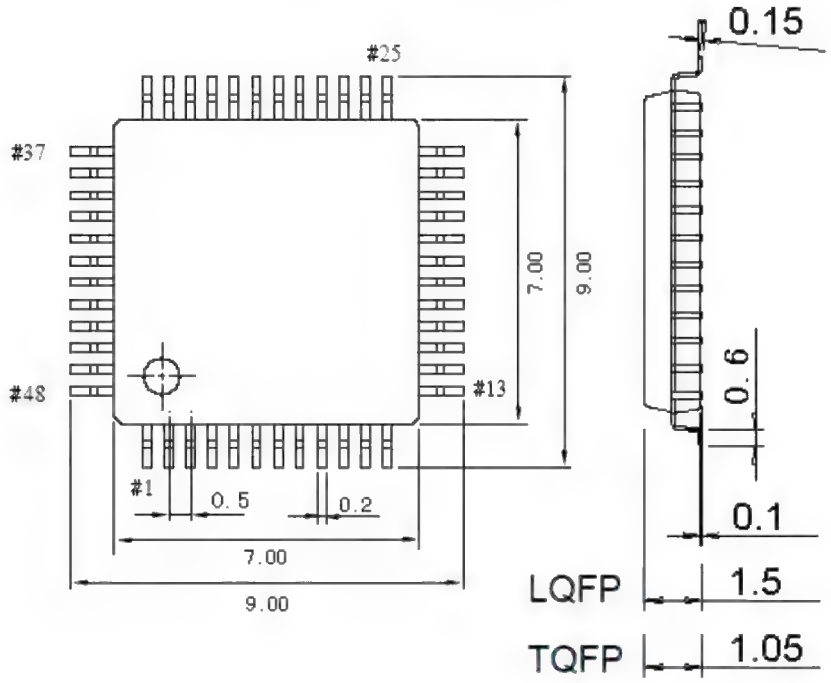


Figure 4-2 QFN48X7_A package

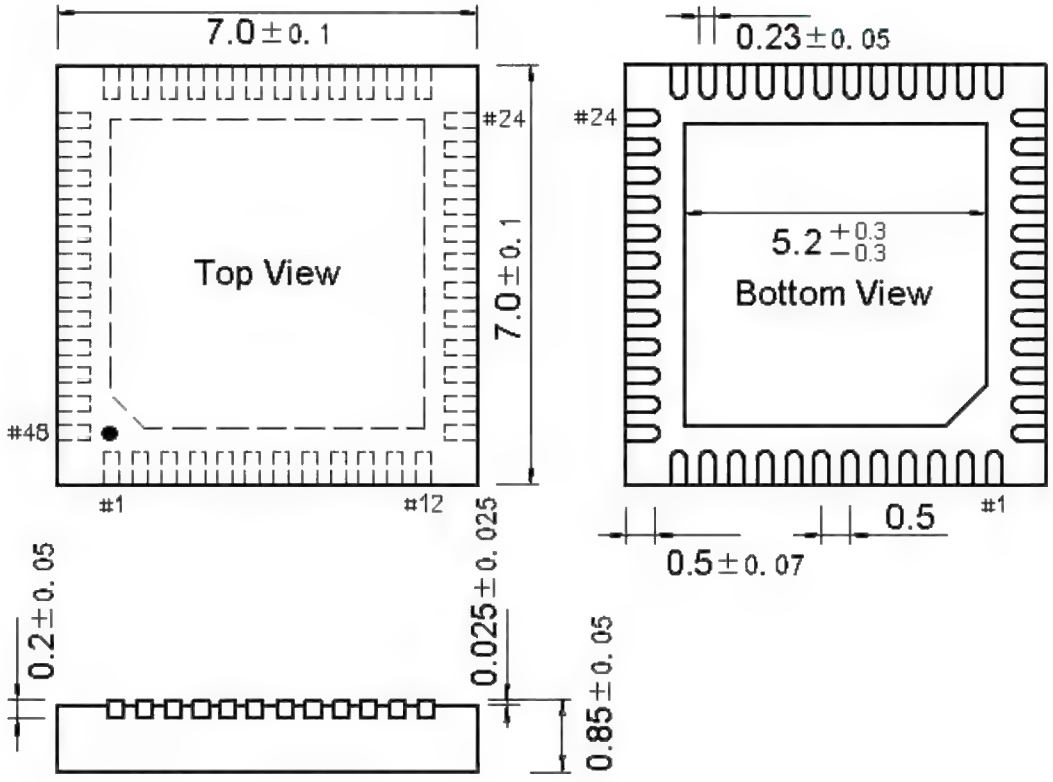


Figure 4-3 QFN48 package

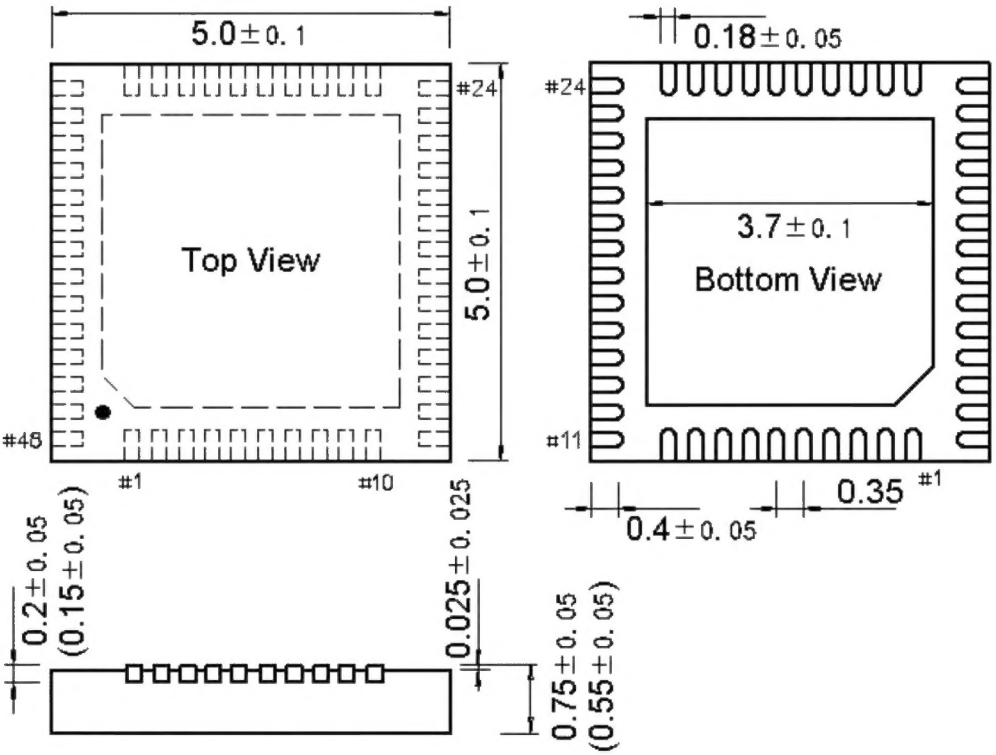


Figure 4-4 QFN32 package

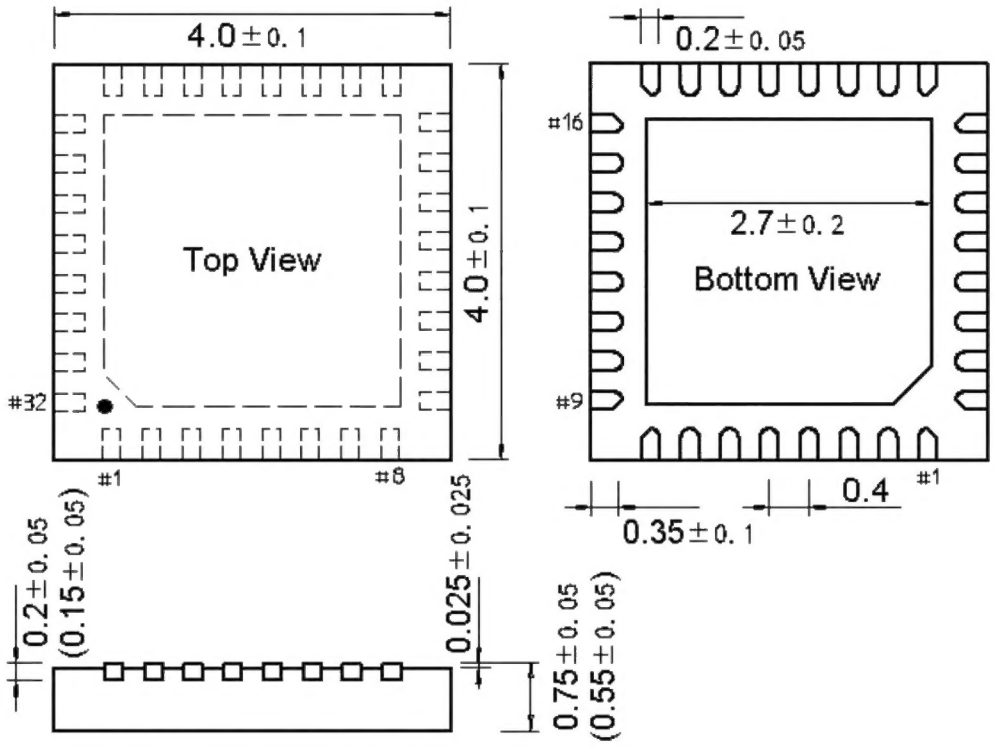
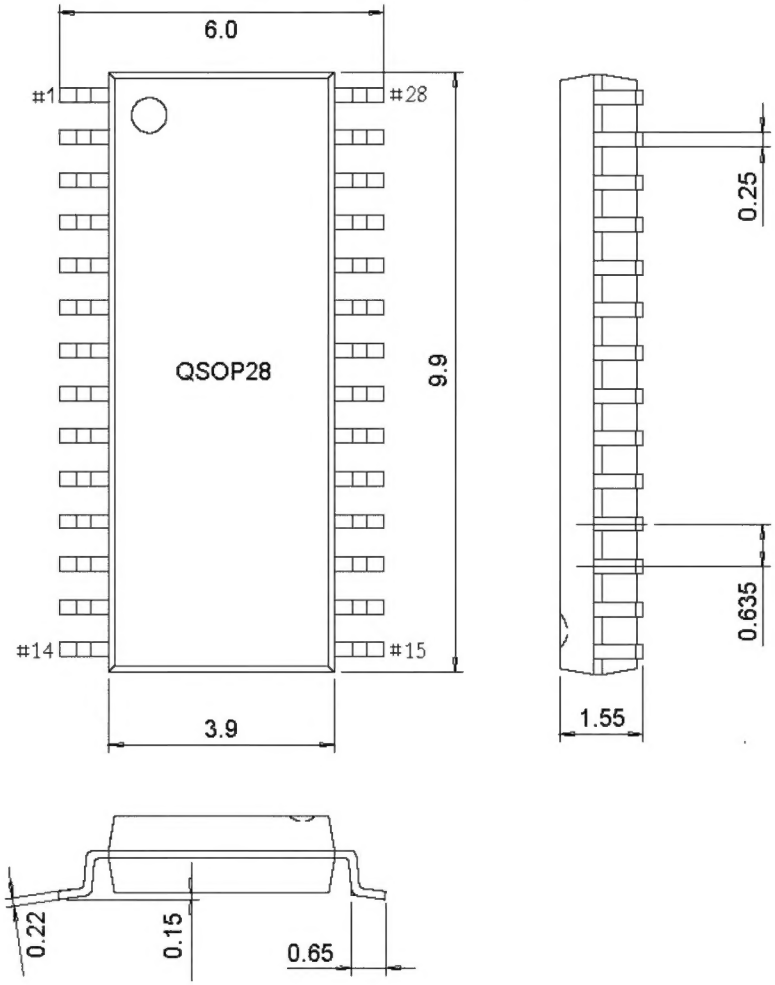


Figure 4-5 QSOP28 package



Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Device family

F = Arm core, general-purpose MCU

V = QingKe RISC-V core, general-purpose MCU

L = QingKe RISC-V core, low-power MCU

X = QingKe RISC-V core, dedicated or special peripherals MCU

M = QingKe RISC-V core, built-in pre-drive motor MCU

Product type (*) + product subseries (*)

Product type	Product subseries
0 = QingKe V2/V4 core, Super value version, system frequency <=48M	02 = 16K Flash memory super value general-purpose 03 = 16K Flash basic general-purpose, OPA 05 = 32K Flash enhanced general-purpose, OPA, dual serial port 06 = 64K Flash versatile, OPA, dual serial port, TKey 07 = Basic motor application, OPA+CMP 35 = Connection, USB, USB PD/Type-C 33 = Connection, USB
1 = M3/QingKe V3/V4 core, Basic version, system frequency<=96M 2 = M3/QingKe V4 non-floating-point core, Enhanced, system frequency <=144M	03 = Connection, USB 05 = Connection, USB HS, SDIO, CAN 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 17 = Interconnected, USB HS, CAN, Ethernet (built-in PHY), SDIO, FSMC

3 = QingKe V4F floating-point core, Enhanced, system frequency <=144M	

Pin number

J = 8 pins D = 12 pins A = 16 pins F = 20 pins E = 24 pins

G = 28 pins K = 32 pins T = 36 pins C = 48 pins R = 64 pins

W = 68 pins V = 100 pins Z = 144 pins

Flash memory size

4 = 16K Flash memory 6 = 32K Flash memory 7 = 48K Flash memory

8 = 64K Flash memory B = 128K Flash memory C = 256K Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40℃~85℃ (Industrial-grade) 7 = -40℃~105℃ (Extended industrial grade, automotive-grade 2)

3 = -40℃~125℃ (Automotive-grade 1) D = -40℃~150℃ (Automotive-grade 0)